1. Class-A Source Follower with External Resistor Output Stage

![Class-A Amplifier Diagram]

Class-A source follower amplifier with external resistor is shown in Figure 1. The current of transistor M1 is given by:

$$I_{DS1} = I_{SS} + \frac{V_o}{R_L}$$

The minimum output voltage $V_o$ occurs when the M1 is cutoff or $I_{DS1} = 0$. That is,

$$V_o (\text{min}) = -I_{SS}R_L$$

If one wants the minimum output voltage to swing to the negative supply rail voltage $V_o (\text{min}) = V_{SS} = -V_{DD} = -5$, the bias current must be selected as follows:

$$I_{SS} = \frac{-V_{SS}}{R_L} = \frac{5}{2K} = 2.5 \text{mA}$$

The output voltage is approximately given by:

$$V_o \approx V_{DD} \sin(wt)$$

The bias voltage, $V_B$, of M1 must be selected so that when the input voltage is zero the current of M1 is equal to $I_{SS} = 2.5 \text{mA}$. That is, class-A Amplifier conducts all the time.

It will be shown that class-A Amplifier is only 25% efficient. The efficiency of the amplifier is defined as the power delivered to the load at the signal frequency, divided by the average power supplied to the amplifier.
\[ eff = \frac{P_{ac}}{P_{av}} \]

The power delivered to the load at the signal frequency is

\[ P_{ac} = \frac{\left( \frac{V_{DD}}{\sqrt{2}} \right)^2}{R_L} = \frac{V_{DD}^2}{2R_L} \]

The average power supplied to the source follower is

\[
\begin{align*}
    P_{av} & = \frac{1}{T} \int_0^T \left[ \frac{I_{SS} (V_{DD} - V_{SS}) + \left( \frac{V_{DD} \sin(wt)}{R_L} \right) V_{DD}}{2} \right] dt \\
        & = I_{SS} (V_{DD} - V_{SS}) = 2I_{SS} V_{DD}
\end{align*}
\]

where \( T \) is the period of signal. The first term corresponds to the dc power dissipation; the second term is the ac power dissipation which average to zero over the period \( T \). The efficiency can now be obtained.

\[ eff = \frac{P_{ac}}{P_{av}} = \frac{V_{DD}^2}{2I_{SS} V_{DD}} = 0.25 \text{ or } 25\% \]

The class-A amplifier is simulated. The netlist is shown below:

```plaintext
* Class A Amplifier
*Filename="classa.cir"
VI 1 5 DC 0 sin(0 5 1000)
VB 5 0 1.4
VDD 3 0 DC 5
VSS 4 0 DC -5
ISS 2 4 2.5mA
M1 3 1 2 4 N1 W=1500U L=2U
RL 2 0 2K
.MODEL N1 NMOS VTO=1 KP=40U
.MODEL P1 PMOS VTO=-1 KP=15U
.OP
.DC VI -5 5 0.05
.TF V(2) VI
.TRAN 1U 2M
.PROBE
.END
```

The DC output voltage transfer characteristic shows linear response for the entire input range.
The current at quiescent operating point is the same as the current source $I_{SS}$. That is, high power dissipation at the quiescent operating point.
The transient analysis shows that with the proper choice of biasing current $I_{SS}$ for given a resistor load, the output voltage can swing the full power supply range.

![Image](image.png)

In this configuration since the source is the output node, the bulk can not be connected to the source for NMOS device in an nwell process. The threshold voltage becomes dependent on the body effect. In the above simulation the effect of non-zero bulk source potential is ignored. The bulk source potential will increase the threshold voltage as shown below:

$$V_T = V_{TO} + \gamma \sqrt{2\phi_F + V_{SB} - \sqrt{2\phi_F}} \approx V_{TO} + \gamma \sqrt{V_{SB}} \approx V_{TO} + \gamma \sqrt{V_O - V_{SS}}$$

It will be shown that the increase in the threshold voltage will decrease the maximum output voltage swing. From Figure 1 the output voltage is given by:

$$V_O = V_I - V_{GS1}$$

The maximum output occurs when the input voltage is set to maximum and gate to source voltage to minimum. That is,

$$V_O(\text{max}) = V_{DD} - V_T \quad \text{since} \quad V_I(\text{max}) = V_{DD}, \quad V_{GS1}(\text{min}) = V_T$$

Substitute the threshold voltage and solve for the maximum output voltage,

$$V_O(\text{max}) = V_{DD} - V_{TO} - \gamma \sqrt{V_O - V_{SS}}$$

Re-arranging the expression,

$$\gamma \sqrt{V_O(\text{max}) - V_{SS}} = V_{DD} - V_{TO} - V_O(\text{max})$$
Squaring both sides and express as polynomial in \( V_o(\text{max}) \)

\[
\gamma^2 (V_o(\text{max}) - V_{SS}) = (V_{DD} - V_{TO} - V_o(\text{max}))^2 = (V_{DD} - V_{TO})^2 - 2V_o(\text{max})(V_{DD} - V_{TO}) + V_o(\text{max})^2
\]

\[aV_o(\text{max})^2 + bV_o(\text{max}) + c = 0\]

where:

\[
a = 1
\]

\[
b = -2(V_{DD} - V_{TO} + \gamma^2 / 2)
\]

\[
c = (V_{DD} - V_{TO})^2 + \gamma^2 V_{SS}
\]

Applying the quadratic formula to solve for the maximum output voltage.

\[
V_o(\text{max}) = V_{DD} + (\gamma^2 / 2) - V_{TO} - (\gamma^2)\sqrt{\gamma^2 + 4(V_{DD} - V_{SS} - V_{TO})}
\]

For the circuit in Figure 1, \( V_{DD} = -V_{SS} = 5 \); \( V_{TO} = 1 \); \( \gamma = \text{GAMMA} = 1 \), the maximum output voltage is computed:

\[
V_o(\text{max}) = 5 + (1^2 / 2) - 1 - (1/2)\sqrt{1^2 + 4(5 - (-5) - 1)} = 1.4586
\]

This is simulated using Pspice with bulk to source voltage parameter GAMMA included.

\[
V_o(\text{max}) = 2.06
\]

That is, one disadvantage of source follower is that the output voltage can not reach the positive voltage rail of VDD cause by high threshold due to non-zero bulk to source voltage. This is simulated by adding the bulk effect SPICE parameter of GAMMA=1.0 and PHI=0.6 in the netlist.

* Class A Amplifier
*Filename="classa.cir" including bulk effect
VI 1 5 DC 0 sin(0 5 1000)
VB 5 0 1.4
VDD 3 0 DC 5
VSS 4 0 DC -5
ISS 2 4 2.5mA
M1 3 1 2 4 NMOS1 W=1500U L=2U
RL 2 0 2K
* SPICE Parameters
.MODEL NMOS1 NMOS VTO=1 KP=40U GAMMA=1.0 PHI=0.6
.OP
.DC VI -5 5 .05
.TF V(2) VI
.TRAN 1U 2M
.PROBE
.END
2. Class-B Push-Pull Source Follower Output Stage

Class-B amplifiers improve the efficiency of the output stage by eliminating quiescent power dissipation by operating at zero quiescent current. This is implemented in Figure 2. As the input voltage $V_i$ swings positive, M1 turns on when $V_{GS1}$ exceeds the threshold voltage $V_{TN1}$, and the output voltage $V_o$
follows the input on the positive swing. When the input voltage $V_i$ swings negative, M2 turns on when $V_{GS2}$ is less than threshold voltage $V_{TP2}$, and the output voltage $V_O$ follows the input on the negative swing. There is a “dead zone” in the class-B voltage transfer characteristic, where both transistors are not conducting, $V_O = 0$. In the dead zone, $V_{GS} = V_{GS1} = V_{GS2} = V_i - V_O = V_i$. That is, the dead zone is defined by:

$$-1 = V_{TP2} \leq V_i \leq V_{TN1} = 1$$

The class-B amplifier is simulated and its netlist is shown below:

* Class B Amplifier
* Filename="classb.cir"
VI 1 0 DC 0 sin(0 5 1000)
VDD 3 0 DC 5
VSS 4 0 DC -5
M1 3 1 2 4 N1 W=1000U L=2U
M2 4 1 2 3 P1 W=4000U L=2U
RL 2 0 2K
.MODEL N1 NMOS VTO=1 KP=40U
.MODEL P1 PMOS VTO=-1 KP=15U
.OP
.DC VI -5 5 .05
.TF V(2) VI
.TRAN 1U 2M
.PROBE
.END

The Pspice simulation shows the presence of the dead zone in the output voltage transfer characteristic.
The current in each transistor conducts for less than half cycle. M1 conducts in the positive half cycle and M2 in the negative half cycle.

The transient analysis shows that the dead zone causes a distortion in the output waveform.
If the cross-over distortion is neglected, then the current flowing in each transistor can be approximated by a half-wave rectified sinusoid with an amplitude of approximately \( V_{DD} / R_L \). Assuming \( V_{DD} = -V_{SS} \), the average power dissipated from each supply is

\[
P_{av} = \frac{1}{T} \int_{0}^{T/2} \frac{V_{DD}}{R_L} V_{DD} \sin \frac{2\pi}{T} t \, dt = \frac{V_{DD}^2}{\pi R_L}
\]

The power delivered to load is the same as in class-A Amplifier. Combining the expression the efficiency is

\[
eff = \frac{P_{ac}}{P_{av}} = \frac{2R_L}{2 \frac{V_{DD}^2}{\pi R_L}} = \frac{\pi}{4} = 0.785 \text{ or } 78.5\%
\]

Pspice can be used to simulate distortion using transient analysis and the .FOUR (Fourier) statement. The syntax is:

```
.FOUR FREQ V1 V2 V3 ...
```

where: FREQ is the frequency of the fundamental

V1 V2 V3 .. are the outputs of the circuit for which Pspice will calculate distortion.

* Class B Amplifier
* Filename="classb.cir" with Fourier Analysis
  .FOUR 1k V(1) V(2)
VI 1 0 DC 0 sin(0 5 1000)
VDD 3 0 DC 5
VSS 4 0 DC -5
M1 3 1 2 4 N1 W=1000U L=2U
M2 4 1 2 3 P1 W=4000U L=2U
RL 2 0 2K
.MODEL N1 NMOS VTO=1 KP=40U
.MODEL P1 PMOS VTO=-1 KP=15U
.OP
.DC VI -5 5 .05
.TF V(2) VI
.TRAN 10U 2M 0 10U
.PROBE
.END

FOURIER COMPONENTS OF TRANSIENT RESPONSE V(1)

DC COMPONENT = 5.009575E-06

<table>
<thead>
<tr>
<th>HARMONIC FREQUENCY</th>
<th>FOURIER COMPONENT</th>
<th>NORMALIZED COMPONENT</th>
<th>PHASE (DEG)</th>
<th>NORMALIZED PHASE (DEG)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 1.000E+03</td>
<td>4.998E+00</td>
<td>1.000E+00</td>
<td>2.511E-04</td>
<td>0.000E+00</td>
</tr>
<tr>
<td>2 2.000E+03</td>
<td>7.521E-07</td>
<td>1.505E-07</td>
<td>-7.954E+01</td>
<td>-7.954E+01</td>
</tr>
<tr>
<td>3 3.000E+03</td>
<td>1.006E-06</td>
<td>2.013E-07</td>
<td>8.401E+01</td>
<td>8.401E+01</td>
</tr>
<tr>
<td>4 4.000E+03</td>
<td>1.512E-06</td>
<td>3.024E-07</td>
<td>8.672E+01</td>
<td>8.672E+01</td>
</tr>
<tr>
<td>5 5.000E+03</td>
<td>1.609E-06</td>
<td>3.220E-07</td>
<td>8.695E+01</td>
<td>8.695E+01</td>
</tr>
<tr>
<td>6 6.000E+03</td>
<td>1.844E-06</td>
<td>3.689E-07</td>
<td>8.867E+01</td>
<td>8.867E+01</td>
</tr>
<tr>
<td>7 7.000E+03</td>
<td>1.759E-06</td>
<td>3.520E-07</td>
<td>8.818E+01</td>
<td>8.818E+01</td>
</tr>
<tr>
<td>8 8.000E+03</td>
<td>1.877E-06</td>
<td>3.755E-07</td>
<td>8.988E+01</td>
<td>8.988E+01</td>
</tr>
<tr>
<td>9 9.000E+03</td>
<td>1.895E-06</td>
<td>3.792E-07</td>
<td>8.954E+01</td>
<td>8.954E+01</td>
</tr>
</tbody>
</table>

TOTAL HARMONIC DISTORTION = 8.961837E-05 PERCENT

FOURIER COMPONENTS OF TRANSIENT RESPONSE V(2)

DC COMPONENT = -2.408525E-02

<table>
<thead>
<tr>
<th>HARMONIC FREQUENCY</th>
<th>FOURIER COMPONENT</th>
<th>NORMALIZED COMPONENT</th>
<th>PHASE (DEG)</th>
<th>NORMALIZED PHASE (DEG)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 1.000E+03</td>
<td>3.330E+00</td>
<td>1.000E+00</td>
<td>-1.172E-02</td>
<td>0.000E+00</td>
</tr>
<tr>
<td>2 2.000E+03</td>
<td>1.679E-02</td>
<td>5.040E-03</td>
<td>8.995E+01</td>
<td>8.996E+01</td>
</tr>
<tr>
<td>3 3.000E+03</td>
<td>4.118E-01</td>
<td>1.237E-01</td>
<td>-1.799E+02</td>
<td>-1.799E+02</td>
</tr>
<tr>
<td>4 4.000E+03</td>
<td>5.550E-03</td>
<td>1.666E-03</td>
<td>8.971E+01</td>
<td>8.972E+01</td>
</tr>
<tr>
<td>5 5.000E+03</td>
<td>2.003E-01</td>
<td>6.014E-02</td>
<td>-1.799E+02</td>
<td>-1.799E+02</td>
</tr>
<tr>
<td>6 6.000E+03</td>
<td>2.419E-03</td>
<td>7.263E-04</td>
<td>8.917E+01</td>
<td>8.918E+01</td>
</tr>
<tr>
<td>7 7.000E+03</td>
<td>1.094E-01</td>
<td>3.286E-02</td>
<td>-1.799E+02</td>
<td>-1.799E+02</td>
</tr>
<tr>
<td>8 8.000E+03</td>
<td>9.528E-04</td>
<td>2.861E-04</td>
<td>8.785E+01</td>
<td>8.786E+01</td>
</tr>
<tr>
<td>9 9.000E+03</td>
<td>5.909E-02</td>
<td>1.774E-02</td>
<td>1.800E+02</td>
<td>1.800E+02</td>
</tr>
</tbody>
</table>

TOTAL HARMONIC DISTORTION = 1.425892E+01 PERCENT
3. Class-AB Amplifiers

The cross-over distortion of the class-B amplifier can be minimized by biasing the transistors into conduction but at a relatively low quiescent current compared to class-A amplifier. This amplifier is known as class-AB and its implementation is shown in Figure 3. Two biasing voltages are shown. At quiescent operating point, both node 5 and node 2 are at ground potential. Thus VGG1 and VGG2 are used to bias M1 and M2 respectively. The two voltages are used to account for the differences in the threshold voltage of the NMOS and PMOS transistors. Ignoring the bulk effect, to guarantee that both transistors are on at quiescent operating point (VI=0), a threshold voltage of 10% beyond VTO(=1) is selected. That is, VGG1=VGG2=1.1V. In the Pspice simulation, the bulk effect is ignored by excluding the parameter GAMMA in the spice parameter list or GAMMA=0. The Pspice netlist of Figure 3 is shown below:

```
* Class AB Amplifier
*Filename=classab.cir"
VI 5 0 DC 0 sin(0 5 1000)
VDD 3 0 DC 5
VSS 4 0 DC -5
VGG1 1A 5 DC 1.1
VGG2 5 1B DC 1.1
M1 3 1A 2 4 N1 W=1500U L=2U
M2 4 1B 2 3 P1 W=4000U L=2U
RL 2 0 2K
*Spice parameter ignoring bulk effect (GAMMA=0)
.MODEL N1 NMOS VTO=1 KP=40U
.MODEL P1 PMOS VTO=-1 KP=15U
.OP
.DC VI -5 5 .05
.TF V(2) VI
.TRAN 1U 2M
.PROBE
```
The DC transfer characteristic of the transistors shows that there is a small bias current of 150uA at quiescent operating point (VI=0). Transistor M1(M2) does not conduct when the input signal VI is negative (positive). Transistor M1(M2) is capable of sourcing(sinking) 2.5mA to the load when the input signal is at the highest possible value of VDD(VSS). That is, class-AB amplifier provides high driving capability at low quiescent operating power. In addition, the cross-over distortion is eliminated by proper selection of bias voltages.

The output voltage DC transfer characteristic shows the elimination of the cross-over distortion.
The transient response shows that the output VO closely follows the input VI, when the bulk effect is ignored. It will shown later that this is not case when the bulk effect is taken into account.
The circuit implementation will become simpler if the input can be moved out of the center tap position as shown in Figure 4. The two bias voltages $V_{GG1}$ and $V_{GG2}$ ignoring bulk effect are combined to $V_{GG}=2.2$. If the bulk effect is ignored and the assumption of equal VTO for both NMOS and PMOS transistors hold, then the movement of the input voltage out of the center tap position requires a bias voltage $VB=-V_{GG}/2=V_{GG2}=-1.1$. It can be shown that Figure 3 and Figure 4 are identical.

Figure 4 Simulation
* Class AB Amplifier
*Filename=”classab2.cir”
VI 1B 5 DC 0 sin(0 5 1000)
VB 5 0 DC -1.1
VDD 3 0 DC 5
VSS 4 0 DC -5
VGG 1A 1B DC 2.2
M1 3 1A 2 4 N1 W=1500U L=2U
M2 4 1B 2 3 P1 W=4000U L=2U
RL 2 0 2K
.Model N1 NMOS VTO=1 KP=40U
.Model P1 PMOS VTO=-1 KP=15U
.OP
.DC VI -5 5 .05
.TF V(2) VI
.TRAN 1U 2M
.PROBE
.END
The voltage, VGG, can be generated by passing a constant current to a resistor RG. The value is selected such that VGG = (RG)(IG). For this example, VGG = 2.2V and IG = 100uA, the value of RG is 22K.

Figure 5 Implementation
* Class AB Amplifier
*Filename="classab3.cir"
VI 1B 5 DC 0 sin(0 5 1000)
VB 5 0 DC -1.1
VDD 3 0 DC 5
VSS 4 0 DC -5
IG 3 1A 100U
RG 1A 1B 22K
M1 3 1A 2 4 N1 W=1500U L=2U
M2 4 1B 2 3 P1 W=4000U L=2U
RL 2 0 2K
.MODEL N1 NMOS VTO=1 KP=40U
.MODEL P1 PMOS VTO=-1 KP=15U
.OP
.DC VI -5 5 .05
.TF V(2) VI
.TRAN 1U 2M
.PROBE
.END
The resistor RG can be implemented using a diode connected transistor M3 as shown in Figure 6. The VGS of M3 is adjusted by selecting the (W/L) of M3 such that $V_{GS3}=V_{GG}$. This is illustrated as follows:

$$I_{DS} = \left(\frac{K_N}{2}\right)\left(\frac{W}{L}\right)(V_{GS} - V_{TN})^2; \text{ since } G = D$$

$$I_G = \left(\frac{K_N}{2}\right)\left(\frac{W}{L}\right)(V_{GS} - V_{TN})^2; \text{ since } I_{DS} = I_G; V_{DS} = V_{GG}$$

$$\left(\frac{W}{L}\right) = \frac{2I_{DS}}{K_N(V_{GS} - V_{TN})^2} = \frac{2(100U)}{(40U)(2.2-1)^2} = 3.47 \approx 3.5$$

This is closely satisfied with a choice of $W=7U$ and $L=2U$. 

Figure 6 Implementation
* Class AB Amplifier
* Filename="classab4.cir" without bulk effect (GAMMA=0)
VI 1B 5 sin(0 5 1000)
VB 5 0 DC -1.1
VDD 3 0 DC 5
VSS 4 0 DC -5
IG 3 1A 100U
M1 3 1A 2 4 N1 W=1500U L=2U
M2 4 1B 2 3 P1 W=4000U L=2U
M3 1A 1B 4 N1 W=7U L=2U
RL 2 0 2K
.MODEL N1 NMOS VTO=1 KP=40U
The three circuits Figure 4, 5 and 6 are simulated with identical results. The transient analysis is shown below to highlight that the current of each transistor is only on for half the cycle. At the crossing point there is a small current flowing in each transistor.
To account for non-symmetric threshold voltages and the bulk effect, a two diode connected transistors are used as shown in Figure 7. The NMOS transistor is used to provide $V_{GG1}$ and the PMOS transistor to provide $V_{GG2}$. The sizing of $M3$ should be the same or less than $M1$. This will guarantee that $V_{GG1} \geq V_{GS1}$. Similarly the size of $M4$ should be the same or less than $M2$.

Figure 7 implementation
* Class AB Amplifier
*Filename="classab5.cir" without bulk effect (GAMMA=0)
VI 1B 6 sin(0 5 1000)
VB 6 0 DC -1.1
VDD 3 0 DC 5
VSS 4 0 DC -5
IG 3 1A 100U
M1 3 1A 2 4 N1 W=1500U L=2U
M2 4 1B 2 3 P1 W=4000U L=2U
M3 1A 1B 5 4 N1 W=1500U L=2U
M4 1B 1B 5 3 P1 W=4000U L=2U
RL 2 0 2K
.MODEL N1 NMOS VTO=1 KP=40U
.MODEL P1 PMOS VTO=1 KP=15U
.OP
.DC VI -5 5 .05
.TF V(2) VI
.TRAN 1U 2M
.PROBE
.END
To study the bulk effect, Figure 6 and 7 are simulated with bulk effect parameter GAMMA included in the SPICE parameter list. Simulation shows that Figure 6 fails to track the threshold voltage VGG needed to cause a class-AB operation, resulting cross-over distortion or class-B operation. While Figure 7 still operates as class-AB amplifier.

* Figure 6 Class AB Amplifier
*Filename="classab4.cir"
VI 1B 5 sin(0 5 1000)
VB 5 0 DC -1.1
VDD 3 0 DC 5
VSS 4 0 DC -5
IG 3 1A 100U
M1 3 1A 2 4 N1 W=1500U L=2U
M2 4 1B 2 3 P1 W=4000U L=2U
M3 1A 1A 1B 4 N1 W=7U L=2U
RL 2 0 2K
*SPICE parameter including bulk effect (GAMMA<>0)
.MDLE N1 NMOS VTO=1 KP=40U GAMMA=1.0
.MDLE P1 PMOS VTO=-1 KP=15U GAMMA=1.0
.OF
.DC VI -5 5 .05
.TF V(2) VI
.TRAN 1U 2M
.PROBE
.END

Figure 6 DC transfer characteristic shows cross-over distortion or class-B operation.
* The input bias voltage need to be adjusted to provide zero output for zero input.

* Class AB Amplifier

V1 1B 6 sin(0 5 1000)

* Figure 7 including bulk effect

Figure 7 DC transfer characteristic shows linear characteristic or class-AB operation but with shifting.
The shifting of the DC transfer characteristic indicates that the input bias voltage VB is no longer correct, when the bulk effect is taken into account. The GAMMA=1.0 for the NMOS and GAMMA=1.0 for the PMOS means that selecting VB=-VGG/2 does not hold. The input bias voltage, VB, must be set to cause the zero output voltage when the input voltage is zero, simulation shows that VB=-1.1-1.57=-2.67 to achieve this.

Figure 7 including bulk effect
*Class AB Amplifier
*Filename="classab5.cir"
VI 1B 6 sin(0 5 1000)
* The input bias voltage need to be adjusted to provide zero output for zero input.
VB 6 0 DC -2.67
VDD 3 0 DC 5
VSS 4 0 DC -5
IG 3 1A 100U
M1 3 1A 2 4 N1 W=1500U L=2U
M2 4 1B 2 3 P1 W=4000U L=2U
M3 1A 1A 5 4 N1 W=1500U L=2U
M4 1B 1B 5 3 P1 W=4000U L=2U
RL 2 0 2K
* SPICE parameter include the bulk effect parameter GAMMA
.MODEL N1 NMOS VTO=1 KP=40U GAMMA=1.0
.MODEL P1 PMOS VTO=-1 KP=15U GAMMA=1.0
.OP
.DC VI -5 .05
.TF V(2) VI
.TRAN 1U 2M
.PROBE
.END
Re-adjusting the input bias voltage $VB$ to center the output voltage DC transfer characteristic.

To study how to achieve the desired output impedance. The current mirror principle can be applied. Note $(W/L)$ can not be independently adjusted. To increase the current in $M1$ and $M2$ by $k$ times requires that $(W/L)_1 = k(W/L)_3$ and $(W/L)_2 = k(W/L)_4$

**** MOSFETS

<table>
<thead>
<tr>
<th>NAME</th>
<th>M1</th>
<th>M2</th>
<th>M3</th>
<th>M4</th>
</tr>
</thead>
<tbody>
<tr>
<td>MODEL</td>
<td>N1</td>
<td>P1</td>
<td>N1</td>
<td>P1</td>
</tr>
<tr>
<td>ID</td>
<td>1.00E-04</td>
<td>-1.00E-04</td>
<td>1.00E-04</td>
<td>-1.00E-04</td>
</tr>
<tr>
<td>VGS</td>
<td>2.67E+00</td>
<td>-2.67E+00</td>
<td>2.67E+00</td>
<td>-2.67E+00</td>
</tr>
<tr>
<td>VDS</td>
<td>5.00E+00</td>
<td>-5.00E+00</td>
<td>2.67E+00</td>
<td>-2.67E+00</td>
</tr>
<tr>
<td>VBS</td>
<td>-5.00E+00</td>
<td>5.00E+00</td>
<td>-5.00E+00</td>
<td>5.00E+00</td>
</tr>
<tr>
<td>VTH</td>
<td>2.59E+00</td>
<td>-2.59E+00</td>
<td>2.59E+00</td>
<td>-2.59E+00</td>
</tr>
<tr>
<td>VDSAT</td>
<td>8.17E-02</td>
<td>-8.17E-02</td>
<td>8.17E-02</td>
<td>-8.17E-02</td>
</tr>
<tr>
<td>GM</td>
<td>2.45E-03</td>
<td>2.45E-03</td>
<td>2.45E-03</td>
<td>2.45E-03</td>
</tr>
<tr>
<td>GDS</td>
<td>0.00E+00</td>
<td>0.00E+00</td>
<td>0.00E+00</td>
<td>0.00E+00</td>
</tr>
<tr>
<td>GMB</td>
<td>5.17E-04</td>
<td>5.18E-04</td>
<td>5.17E-04</td>
<td>5.18E-04</td>
</tr>
</tbody>
</table>

**** SMALL-SIGNAL CHARACTERISTICS

$V(2)/VI = 8.255E-01$

INPUT RESISTANCE AT $VI = 2.150E+11$
OUTPUT RESISTANCE AT $V(2) = 1.685E+02$
*Class AB Amplifier
*Filename="classab5.cir"

VI 1B 6 sin(0 5 1000)
VB 6 0 DC -2.67
VDD 3 0 DC 5
VSS 4 0 DC -5
IG 3 1A 100U
M1 3 1A 2 4 N1  W=1500U L=2U
M2 4 1B 2 3 P1  W=4000U L=2U
M3 1A 1 5 4 N1 W=150U L=2U
M4 1B 1B 5 3 P1 W=400U L=2U
*RL 2 0 2k

*.MODEL N1 NMOS VTO=1 KP=40U GAMMA=1.0
*.MODEL P1 PMOS VTO=-1 KP=15U GAMMA=1.0
.OP
.DC VI -5 5 .05
.TF V(2) VI
.TRAN 1U 2M
.PROBE
.END

**** MOSFETS

<table>
<thead>
<tr>
<th>NAME</th>
<th>M1</th>
<th>M2</th>
<th>M3</th>
<th>M4</th>
</tr>
</thead>
<tbody>
<tr>
<td>MODEL</td>
<td>N1</td>
<td>P1</td>
<td>N1</td>
<td>P1</td>
</tr>
<tr>
<td>ID</td>
<td>1.00E-03</td>
<td>-1.00E-03</td>
<td>1.00E-04</td>
<td>-1.00E-04</td>
</tr>
<tr>
<td>VGS</td>
<td>2.88E+00</td>
<td>-2.82E+00</td>
<td>2.88E+00</td>
<td>-2.82E+00</td>
</tr>
<tr>
<td>VDS</td>
<td>4.85E+00</td>
<td>-5.15E+00</td>
<td>2.88E+00</td>
<td>-2.82E+00</td>
</tr>
<tr>
<td>VBS</td>
<td>-5.15E+00</td>
<td>4.85E+00</td>
<td>-5.15E+00</td>
<td>4.85E+00</td>
</tr>
<tr>
<td>VTH</td>
<td>2.62E+00</td>
<td>-2.56E+00</td>
<td>2.62E+00</td>
<td>-2.56E+00</td>
</tr>
<tr>
<td>VDSAT</td>
<td>2.58E-01</td>
<td>-2.58E-01</td>
<td>2.58E-01</td>
<td>-2.58E-01</td>
</tr>
<tr>
<td>GM</td>
<td>7.75E-03</td>
<td>7.75E-03</td>
<td>7.75E-04</td>
<td>7.75E-04</td>
</tr>
<tr>
<td>GDS</td>
<td>0.00E+00</td>
<td>0.00E+00</td>
<td>0.00E+00</td>
<td>0.00E+00</td>
</tr>
<tr>
<td>GMB</td>
<td>1.62E-03</td>
<td>1.66E-03</td>
<td>1.62E-04</td>
<td>1.66E-04</td>
</tr>
</tbody>
</table>

**** SMALL-SIGNAL CHARACTERISTICS

\[
\frac{V(2)}{VI} = 8.236E-01
\]

INPUT RESISTANCE AT VI = 2.156E+11

OUTPUT RESISTANCE AT V(2) = 5.329E+01

\[
R_{OP} = R_{O2} = \frac{1}{g_{m2}} = \frac{1}{\sqrt{2K_r(W/L)_{D2}}} = \frac{1}{\sqrt{2(15)(4000U/2U)(1m)}} = 129 \text{ ohm}
\]

\[
R_{ON} = R_{O1} = \frac{1}{g_{ml}} = \frac{1}{\sqrt{2K_N(W/L)_{D1}}} = \frac{1}{\sqrt{2(40)(1500U/2U)(1m)}} = 129 \text{ ohm}
\]

\[
R_O = R_{OP}/R_{ON} = 129/2 = 64.5 \text{ ohm}
\]