Lab 8: 2\textsuperscript{nd} Order Universal Filter Design

Wide-Swing Folded-Cascode OTA Biasing Circuit

\[ \frac{W_n}{L_n} = \frac{(18L}{6L} \quad \frac{W_p}{L_p} = \frac{(54L}{6L} \]

Where the divisor \( n = 7 \)

\[ R = 360k \]

\[ V_{dd}=2.5V \quad V_{ss}=-2.5V \]

\[ V_{TP0} \Delta V_p \quad V_{TN0} \Delta V_N \]

\[ V_{TP} \Delta V_p \quad V_{TN} \Delta V_N \]

\[ (m2) \]

\[ (m3) \]

\[ V_b1=1.3122 \quad V_b2=0.7738 \quad V_b3=-0.70724 \quad V_b4=-1.4295 \]

\[ V_TN^0 \Delta V_N \]

\[ V_{TP} \Delta V_p \]

\[ V_{TP^+} \Delta V_p \]

\[ V_{TN^0} \Delta V_N \]

\[ V_{TN} \Delta V_N \]

\[ V_{TP^+} \Delta V_p \]

10\mu A

Figure 1. Biasing circuit for the wide-swing folded-cascode OTA
In the AFFIRMA simulation, we will be using DC analysis to obtain the biasing voltage as shown above. This is done as follows:

[MENU]Analyses>Choose

Select analyses to be DC and check “Save DC operating point” as shown in figure 2:

![Choosing Analyses](image)

After running the simulation, click [menu]Results -> print -> DC node voltages. The test bench schematic will show up to prompt you to choose which node’s voltage to be displayed. Click on vb1 to vb4 sequentially to display their voltages and compare them to the values given on figure 1.
Wide-Swing Folded-Cascode OTA

*NOTE: All transistors are 3-terminal type (D,G,S) with
NMOS bulk (B) connected to VSS, and
PMOS bulk (B) connected to VDD

(Wn/Ln)=(18L/6L)
(Wp/Lp)=(54L/6L)

Figure 5. Wide-swing folded-cascode OTA
Figure 6: OTA Schematic

Figure 7: OTA Symbol
Second Order Universal Filter Schematic

(a)

(b)

Table:

<table>
<thead>
<tr>
<th>Type</th>
<th>V1</th>
<th>V2</th>
<th>V3</th>
</tr>
</thead>
<tbody>
<tr>
<td>LP</td>
<td>V_i</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>HP</td>
<td>0</td>
<td>V_i</td>
<td>0</td>
</tr>
<tr>
<td>BP</td>
<td>0</td>
<td>0</td>
<td>V_i</td>
</tr>
<tr>
<td>BR</td>
<td>V_i</td>
<td>V_i</td>
<td>0</td>
</tr>
</tbody>
</table>

(c) Second order universal filter schematic including biasing circuit, C1=C2=10pf.

Figure 8. Second Order Universal Filter Schematic
Functional Simulation with Affirma

Create a test bench schematic of the filter design with VDC sources connecting to V1, V2, V3, myvdd and myvss, which give myvdd +2.5V and myvss –2.5V but leave V1, V2 and V3 unspecified. The values are to be set during simulation for different filtering cases. In this situation, since we named our pins to be v1, v2 and v3, it is necessary to name the VDC sources to be something else than v1, v2 or v3 (their default names). Otherwise, errors will be given during simulation.

Followed the previous handouts for simulation in Affirma.

1. Setup for AC analysis from 1Hz to 100G.
   [MENU] Analyses > Choose
   [Dialog Box]
   - Select AC
   - Start Freq: 1
   - Stop Freq: 100G
   - Click OK.

2. Apply inputs forces for LPF simulation
   Select the VDC source connected to pin v1,
   Modify its property, set AC Magnitude to be 1 V.

   Select the VDC source connected to pin v2,
   Modify its property, set DC to be 0 V

   Select the VDC source connected to pin v3,
   Modify its property, set DC to be 0 V

3. Choose vout to be plotted.

4. Run the simulation.

You should see simulation as shown in figure 9 on the next page.

5. Setup VDCs for other filter configurations as shown in Figure 8(b) to get simulation results as shown in figure 10, 11, and 12.
Figure 9: Universal Filter with LowPass Configuration

Figure 10: Universal Filter with HighPass Configuration
Figure 11: Universal Filter with BandPass Configuration

Figure 12: Universal Filter with BandReject Configuration
Layout

1. OTA Biasing Circuit

a. OTA Biasing Circuit Schematic for Layout

The above schematic differs from Fig. 2 with the external biasing resistor $R_b$ missing. A pin RIN is provided for connecting $R_b$ externally.

b. OTAbias Symbol

This biasing symbol also differs from the previous symbol with an additional RIN pin available for connecting $R_b$ externally.
c. Biasing Circuit Layout
The height of the layout is about 200 lambda. This height is selected to match up with the OTA layout, so that their VDD and VSS power rails will abut.

2. OTA

a. OTA Schematic for Layout

The schematic is identical to Figure 6.
b. OTA Symbol

This symbol is identical to that in Lab 8a.

![OTA Symbol](image)

Figure 17: OTA Symbol

c. OTA Layout

![OTA Layout](image)

Figure 18: OTA Layout
3. Capacitor

a. Capacitor schematic

Figure 19: Cap10p Schematic

b. Capacitor Symbol

Figure 20: Cap10p Symbol
c. Capacitor Layout

Figure 21: Cap10p Layout
4. Second Order Universal Filter

a. Universal Filter Schematic

(c) Second order universal filter schematic including biasing circuit, C1=C2=10pf.

Figure 22. Second Order Universal Filter Schematic for Layout
b. Filter Symbol

Figure 23: Second Order Universal Filter Symbol for Layout

Figure 24: Second Order Universal Filter Layout Hierarchical View

c. Filter Layout
Figure 25: Second Order Universal Filter Layout Detailed View

You should notice that there is an additional metal power rail at the bottom of this layout, which represents pin mygnd.

DRC and LVS checks need to be performed to avoid any kind of error.
d. Test Bench Creation and Simulation

Figure 26: Post-layout Simulation Test Bench for the Second Order Universal Filter

In Affirma, setup the input voltages as in the pre-layout simulation for LowPass, HighPass, BandPass, and BandReject configurations. You should get the results very close to what you had before.

This concludes the second order universal filter design.