AD CONVERTER

1. 2-BIT AD Using R-2R

Figure 1. 2-BIT AD Schematic Diagram.

*Filename = "AD2R2R.CIR"
*AD 2-bit model

.LIB C:\e595\lib\mybspice.lib
.PARAM R=10K
.PARAM R2=(2*R)

Vth vth 0 DC 5V
VIN vin 0 DC 0V

.xcp0 vin i00 V0 compbuf
.xcp1 vin i10 V1 compbuf

*i10 summing resistors
R11 vth i10 {R2}
R12 0 i10 {R2}

*i00 summing resistors
RF10 V1 i00 {R2}
R01 i01 i00 {R}
R02 i01 vth {R2}
R03 i01 0 {R2}

* Analysis
.DC VIN 0 5 .005
.PROBE
.END

2. 4-BIT AD Using R-2R
Figure 2. 4-BIT AD Schematic Diagram
*Filename = "AD4R2R1.CIR"
.LIB C:\e595\lib\myspice.lib

*AD 4-bit model
.PARAM R=10K
.PARAM R2=(2*R)

Vth vth 0 DC 5V
VIN vin 0 DC 0V

xcp0 vin i00 V0 compbuf
xcp1 vin i10 V1 compbuf
xcp2 vin i20 V2 compbuf
xcp3 vin i30 V3 compbuf

*i30 summing resistors
R31 vth 130 {R2}
R32 0 130 {R2}

*i20 summing resistors
RF32 V3 i20 {R2}
R21 i21 120 {R}
R22 i21 vth {R2}
R23 i21 0 {R2}

*i10 summing resistors
RF31 V3 i10 {R2}
R11 i11 110 {R}
RF21 V2 i11 {R2}
R12 i11 i12 {R}
R13 i12 vth {R2}
R14 i12 0 {R2}

*i00 summing resistors
RF30 V3 i00 {R2}
R01 i01 100 {R2}
RF20 V2 i01 {R2}
R02 i01 102 {R}
RF10 V1 i02 {R2}
R03 i02 103 {R}
R04 i03 vth {R2}
R05 i03 0 {R2}

* Analysis
.DC VIN 0 5 .05
.PROBE
.END
* Netlist for CMOS Comparator in Nwell
M1 5 in- 7 7 PMOS1 W=15U L=6.6U
M2 6 in+ 7 7 PMOS1 W=15U L=6.6U
M3 5 5 4 4 NMOS1 W=5.4U L=6.6U
M4 6 5 4 4 NMOS1 W=5.4U L=6.6U
M5 7 9 3 3 PMOS1 W=30U L=6.6U
M6 outc 6 4 4 NMOS1 W=21.6U L=6.6U
M7 outc 9 3 3 PMOS1 W=60U L=6.6U
M8 9 9 3 3 PMOS1 W=60U L=6.6U
xinv1 outc out1 inv1
xinv3 outc out1 inv3
* External Components
*CL 8 0 2pF
RB 9 0 175K
VDD 3 0 DC 5V
VSS 4 0 DC 0V
.ENDS

.SUBCKT inv1 in out
VDD 3 0 DC 5V
VSS 4 0 DC 0V
M1 out in 4 4 NMOS1 W=3.6U L=1.2U
M2 out in 3 3 PMOS1 W=6.6U L=1.2U
.ENDS

.SUBCKT inv3 in out
VDD 3 0 DC 5V
VSS 4 0 DC 0V
M1 out in 4 4 NMOS1 W=10.8U L=1.2U
M2 out in 3 3 PMOS1 W=19.8U L=1.2U
.ENDS
3. AD Theory of Operation.

Figure 3 shows the negative input circuits of the 4-bit AD. The negative input \(i00\) will be analyzed in detail to derive the AD operation. Figure 4 shows the equivalent circuit transformations as the analysis progresses from the threshold input voltage, \(V_{th}\), toward the comparator negative input voltage source \(V3\). Fig 4(b) converts the \(V_{th}\) source to current source using norton equivalent circuit. This conversions enable us to combine the two resulting resistances in parallel. Then in Figure 4(c), the current source is converted back to voltage source using thevenin equivalent circuit, resulting in two voltage sources \(V_{th}/2\) and \(V1\) in thevenin equivalent forms connected in parallel, which can be combined by converting them to current sources using norton equivalent circuits shown in Figure 4(d). The process is repeated until it is reduced to a single voltage source in Figure 4(g). Following a similar analysis the negative input voltages are summarized below:

\[
\begin{align*}
V_{30} &= V_{th}/2 \\
V_{20} &= V_{th}/4 + V1/2 \\
V_{10} &= V_{th}/8 + V1/4 + V2/2 \\
V_{00} &= V_{th}/16 + V1/8 + V2/4 + V3/2
\end{align*}
\]

Let \(u(x)\) be a step function, \(u=1\) if \(x>0\); 0 otherwise. The output of each comparator for a 4-bit AD can be written as follows:

\[
\begin{align*}
V_3 &= 5u(V_{in} - \frac{V_{th}}{2}) \\
V_2 &= 5u(V_{in} - \frac{V_{th}}{4} - \frac{V_3}{2}) \\
V_1 &= 5u(V_{in} - \frac{V_{th}}{8} - \frac{V_2}{4} - \frac{V_3}{2}) \\
V_0 &= 5u(V_{in} - \frac{V_{th}}{16} - \frac{V_1}{8} - \frac{V_2}{4} - \frac{V_3}{2})
\end{align*}
\]

The output expression for each output of a 2-bit AD can be written as follows:

\[
\begin{align*}
V_1 &= 5u(V_{in} - \frac{V_{th}}{2}) \\
V_0 &= 5u(V_{in} - \frac{V_{th}}{4} - \frac{V_1}{2})
\end{align*}
\]

The above expression can be generalized to:

\[
V_k = 5u(V_{in} - \frac{V_{th}}{2^{N-k}} - \sum_{i=k+1}^{N-1} \frac{V_i}{2^{N-i}})
\]

where : \(N\) is the total number of bits, \(k\) is kth comparator output.

As an example, consider a 4-bit AD with \(V_{th}=5V\). This AD will convert 5V to 1111 and 0V to 0000. What will \(V_{in}=3V\) converts to?
\[ V_3 = 5u(V_{in} - \frac{V_{in}}{2}) = 5u(3 - \frac{5}{2}) = 5 \]

\[ V_2 = 5u(V_{in} - \frac{V_{in}}{4} - \frac{V_{in}}{2}) = 5u(3 - \frac{5}{4} - \frac{5}{2}) = 0 \]

\[ V_1 = 5u(V_{in} - \frac{V_{in}}{8} - \frac{V_2}{4} - \frac{V_3}{2}) = 5u(3 - \frac{5}{8} - \frac{0}{4} - \frac{5}{2}) = 0 \]

\[ V_0 = 5u(V_{in} - \frac{V_{in}}{16} - \frac{V_1}{8} - \frac{V_2}{4} - \frac{V_3}{2}) = 5u(3 - \frac{5}{16} - \frac{0}{8} - \frac{0}{4} - \frac{5}{2}) = 5 \]

That is \( V_{in}=3V \) is mapped to 1001=9 (dec). This can be verified as follows:

\[
\frac{x}{15} = \frac{3}{5} \\
\frac{x}{5} = \frac{3}{15} = 9
\]
Figure 3. The Four Negative Input Circuits (a) – (d) of the 4-BIT AD.
Figure 4. Comparator Negative Input i00 Circuit Transformations (a) – (g) used in Deriving the Equivalent Voltage applied at Input i00.