Common Source Amplifier: NMOS Inverter Amplifier with PMOS Current Load.

Figure 1(a) is a common source amplifier with ideal current source load. Figure 1(b) is its implementation using PMOS with constant gate voltage.

1. Low Frequency Small Signal Equivalent Circuit

Figure 1(c) shows its low frequency equivalent circuit. That is, all the stray capacitances are ignored. The two-port parameters are to be determined. Comparing Figure 1(c) and Figure 1(d), one obtains:

\[ Y_L = g_{ds2} \text{ (or } Z_L = r_{ds2}) \text{; } Y_S = \infty \text{ (or } Z_S = 0) \]

\[ V_1 = V_i = V_{gs1} \]

and

\[ V_2 = V_o \]

From Fig 1, the current equations are derived to obtain the Y parameters:

\[ I_1 = 0 \]

\[ I_2 = g_{ml} V_1 + g_{ds1} V_2 \]

That is, the Y-parameter matrix is given by:

\[ Y = \begin{bmatrix}
0 & 0 \\
g_{ml} & g_{ds1}
\end{bmatrix}; \text{ det}Y = 0 \]

The input impedance of common source circuit,

\[ Z_i = \frac{y_{22} + Y_L}{\text{det}Y + y_{11}Y_L} = \frac{g_{ds1} + g_{dc2}}{0 + (0)g_{dc2}} = \infty \]

The output impedance of the common source circuit,

\[ Z_o = \frac{y_{11} + Y_S}{\text{det}Y + y_{22}Y_S} = \frac{1}{y_{22}} = \frac{1}{g_{ds1}} \]

The dc voltage gain is,

\[ A_{V0} = -\frac{y_{21}}{y_{22} + Y_L} = -\frac{g_{ml}}{g_{ds1} + g_{dc2}} \text{ or} \]

\[ A_{V0} = -g_{ml} \left( Z_o \parallel Z_L \right) = -g_{ml} R_{out} \text{ ; } R_{out} = Z_o \parallel Z_L = \frac{1}{g_{ds1} + g_{dc2}} \]

The current gain is,
$$A_1 = -\frac{y_{21}Y_L}{\text{det}Y + y_{11}Y_L} = -\frac{g_{m1}g_{as2}}{0 + 0} = \infty$$
Figure 1. Common Source Amplifier: (a) ideal current source load, (b) PMOS current source load, (c) low frequency small signal equivalent circuit, and (d) two-port representation.
2. Common Source NMOS Inverter Amplifier with PMOS Current Load Static Static Characteristic

The small signal equivalent circuit assumes that its operating point has been properly set. To achieve this, one needs to determine the static or large signal characteristics of the amplifier. It will be shown that the operating point range for a high gain amplifier is very narrow. Hence, its selection is very critical. A little error will cause the circuit to cease functioning as an amplifier.

Figure 2 shows the various regions of operation for each transistor. It is determined as follows:

MN Transistor Operating Regions:

- **Cutoff**
  \[ V_{GSN} = V_{IN} - V_{SS} < V_{TN} \]
  \[ V_{IN} < V_{TN} + V_{SS} = 1 + (-2.5) = -1.5 \text{V} \]

- **Saturation**
  \[ V_{IN} > -1.5 \]
  and
  \[ V_{GSN} - V_{TN} < V_{DSN} \]
  \[ V_{IN} - V_{SS} - V_{TN} < V_{O} - V_{SS} \]
  \[ V_{IN} - V_{TN} < V_{O} \]
  \[ V_{IN} - 1 < V_{O} \]

- **Ohmic**
  \[ V_{IN} > -1.5 \]
  and
  \[ V_{IN} - V_{TN} > V_{O} \]

MP Transistor (Current Source) Operating Regions:

- **Cutoff**
  \[ |V_{GSP}| = |V_{G} - V_{DD}| < |V_{TP}| \]
  \[ |0 - 2.5| < |-1| \] **Can’t be satisfied \(\Rightarrow\) No cutoff region

- **Saturation**
  \[ |V_{GSP}| - |V_{TP}| < |V_{DSP}| \]
  \[ |V_{G} - V_{DD}| - |V_{TP}| < |V_{O} - V_{DD}| \]
  \[ (V_{DD} - V_{G}) + V_{TP} < (V_{DD} - V_{O}) \]
  \[-V_{G} + V_{TP} < V_{O} \]
  \[ V_{G} - V_{TP} > V_{O} \]
  \[ 0 - (-1) > V_{O} \]
  \[ V_{O} < 1 \]

- **Ohmic**
  \[ V_{O} > 1 \]
These are summarized as follows:

<table>
<thead>
<tr>
<th>Operating Region</th>
<th>MN</th>
<th>MP</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cutoff</td>
<td>(V_{IN}&lt; -1.5)</td>
<td>None</td>
</tr>
<tr>
<td>Saturation</td>
<td>(V_{IN}&gt; -1.5) &amp; (V_{IN} - 1 &lt; V_o)</td>
<td>(V_o &lt; 1)</td>
</tr>
<tr>
<td>Ohmic</td>
<td>(V_{IN}&gt; -1.5) &amp; (V_{IN} - 1 &gt; V_o)</td>
<td>(V_o &gt; 1)</td>
</tr>
</tbody>
</table>

The various regions of operation of inverting amplifier are summarized as follows:

<table>
<thead>
<tr>
<th>Operating Region</th>
<th>MN</th>
<th>MP</th>
</tr>
</thead>
<tbody>
<tr>
<td>Region I</td>
<td>Cutoff</td>
<td>Ohmic</td>
</tr>
<tr>
<td>Region II</td>
<td>Saturation</td>
<td>Ohmic</td>
</tr>
<tr>
<td>Region III</td>
<td>Saturation</td>
<td>Saturation</td>
</tr>
<tr>
<td>Region IV</td>
<td>Ohmic</td>
<td>Saturation</td>
</tr>
<tr>
<td>Region V</td>
<td>Ohmic</td>
<td>No Cutoff, always on</td>
</tr>
</tbody>
</table>

These regions are shown in the in the PSpice transfer characteristic graph.

The common source amplifier circuit is shown in Figure 1(b). The power supplies and netlist used in PSpice simulation and numerical calculations are also indicated. From Figure 1(b), the load current is equal to the driver current, i.e.

\[i_P = i_N\]

The PMOS transistor MP with a constant \(V_{GS}\) behaves as a constant current source. Subscripts P and N are used to distinguish the variables and parameters of the two types of transistors. The current equation of the transistor MP in saturated case is given by:

\[i_r = -(\beta / 2)[\left|V_{GSP} - V_{TP}\right|] \text{ when } \left|V_{GSP} - V_{TP}\right| \leq \left|V_{DS}\right|\]

Substituting for \(V_{GSP} = V_G - V_{DD}\),

\[i_r = (\beta / 2)[\left|V_G - V_{DD}\right| - \left|V_{TP}\right|] \text{ when } \left|V_G - V_{DD}\right| - \left|V_{TP}\right| \leq \left|V_o - V_{DD}\right|\]

The absolute value symbol can be eliminated by accounting for the sign of each term within the symbol. For PMOS transistor the following hold: \(V_G < V_{DD}\), \(V_{TP} < 0\), \(V_o - V_{DD} < 0\).

The above current equation reduces to:

\[i_r = (\beta / 2)[(V_{DD} - V_G) + V_{TP}] \text{ when } (V_{DD} - V_G) + V_{TP} \leq V_{DD} - V_o \text{ or } V_G - V_{TP} > V_o\]

Similarly, the PMOS current equation for the ohmic case is given by:

\[i_P = \beta_p [(V_{GSP} - V_{TP})] \left|V_{DS}\right| - \left|V_{DS}\right|^2 / 2 \text{ when } V_{GSP} - V_{TP} \leq V_o\]

\[i_P = \beta_p [(V_{DD} - V_G + V_{TP})(V_{DD} - V_o) - (V_{DD} - V_o)^2 / 2] \text{ when } V_{GSP} - V_{TP} \leq V_o\]

For the NMOS driver transistor MN current equations are given by:
\[ i_n = \left(\frac{\beta_n}{2}\right)(V_{\text{GSN}} - V_{\text{IN}})^2 \text{ when } V_{\text{GSN}} - V_{\text{IN}} \leq V_{\text{DSN}}, \text{ MN is saturated.} \]

Substituting for \( V_{\text{GSN}} = V_i - V_{\text{SS}}, \) and \( V_{\text{DSN}} = V_O - V_{\text{SS}} \)
\[ i_n = \left(\frac{\beta_n}{2}\right)(V_i - V_{\text{ss}} - V_{\text{IN}})^2 \text{ when } V_i - V_{\text{ss}} - V_{\text{IN}} \leq V_o - V_{\text{ss}} \text{ or } V_i - V_{\text{IN}} \leq V_o, \text{ MN is saturated.} \]

Similarly, the NMOS current equation for the ohmic case is given by:
\[ i_n = \left[ (V_i - V_{\text{ss}} - V_{\text{IN}})(V_o - V_{\text{ss}}) - (V_o - V_{\text{ss}})^2 / 2 \right] \text{ when } V_i - V_{\text{IN}} > V_o, \text{ MN is ohmic.} \]

The static characteristic is determined by equating the corresponding current equations at each voltage range:

1. \( V_i - V_{\text{SS}} < V_{\text{TN}} \text{ and } V_G - V_{\text{TP}} = 0 \text{ (zero)} < 1 < V_o. \text{ The driver transistor MN is off, and MP is on (ohmic). Hence } V_o = V_{\text{dd}}. \)

2. \( V_i - V_{\text{SS}} > V_{\text{TN}}, V_i - V_{\text{TN}} < V_o, \) and \( V_G - V_{\text{TP}} < V_o. \) The driver transistor MN is saturated, and the load transistor MP is ohmic.
\[ (\beta_n / 2)(V_i - V_{\text{ss}} - V_{\text{TN}})^2 = \beta_p [(V_{\text{dd}} - V_G + V_{\text{TP}})(V_{\text{dd}} - V_o) - (V_{\text{dd}} - V_o)^2 / 2] \]

Solving for \( V_o, \)
\[ V_o = (V_G - V_{\text{TP}}) - \sqrt{(V_{\text{dd}} - V_G + V_{\text{TP}})^2 - \beta_R (V_i - V_{\text{ss}} - V_{\text{TN}})^2} \]
where \( \beta_R = \beta_n / \beta_p \)

3. \( V_i - V_{\text{SS}} > V_{\text{TN}}, V_i - V_{\text{TN}} < V_o, \) and \( V_G - V_{\text{TP}} > V_o. \) The driver transistor MN is saturated, and the load transistor MP is also saturated.
\[ (\beta_n / 2)(V_i - V_{\text{ss}} - V_{\text{TN}})^2 = (\beta_p / 2)(V_{\text{dd}} - V_G + V_{\text{TP}})^2 \]
This equation is independent of \( V_o, \) it is used to determine the operating point \( V_{\text{bias}} \) of the inverter.
Solving for \( V_{\text{bias}}, \)
\[ V_i = V_{\text{bias}} = V_{\text{ss}} + V_{\text{TN}} + (V_{\text{dd}} - V_G + V_{\text{TP}}) / \sqrt{\beta_R} \]
This value is only an approximation. The exact value is obtained from the PSpice simulation. The bias voltage corresponds to the input voltage \( V_i \) when the output voltage \( V_o = (V_{\text{dd}} + V_{\text{ss}})/2 = (2.5 + 2.5)/2 = 0. \)

4. \( V_i - V_{\text{SS}} > V_{\text{TN}}, V_i - V_{\text{TN}} > V_o, \) and \( V_G - V_{\text{TP}} > V_o. \) The driver transistor MN is ohmic, and the load transistor MP is saturated.
\[ \beta_n [(V_i - V_{\text{ss}} - V_{\text{TN}})(V_o - V_{\text{ss}}) - (V_o - V_{\text{ss}})^2 / 2] = (\beta_p / 2)(V_{\text{dd}} - V_G + V_{\text{TP}})^2 \]
Solving for \( V_o, \)
\[ V_o = (V_i - V_{\text{TN}}) - \sqrt{(V_i - V_{\text{ss}} - V_{\text{TN}})^2 - (V_{\text{dd}} - V_G + V_{\text{TP}})^2 / \beta_R} \]

5. \( V_o = V_{\text{SS}}, \) when the load transistor MP is off. It occurs when \( V_{\text{GSP}} = V_G - V_{\text{DD}} > V_{\text{TP}}. \) But for the given \( V_G = 0 \) this can not happen. This is verified in the Pspice simulation.
Figure 2 shows that \( V_{\text{SS}} = -2.5 \text{ V can never be reached.} \)
For the given parameters, the operating point $V_{bias}$ is computed for the given example. The W/L ratio must use the $L_{eff} = L - 2*LD = 5.4u - 2*(0.5u) = 4.4u$. 

Figure 2. The various operating regions of nmos common source amplifier with pmos current load
The bias point from PSpice simulation is 7.6205mV reasonably closed to the calculated value of 0. From the transfer characteristic graph, a bias voltage of 0 is a reasonably good choice, it will be used in the subsequent experiments.

Figure 1(c) shows the low frequency small signal equivalent circuit. The small signal dc gain is given in section 1, as

\[ A_{v0} = -g_{mN} R_{out} \]

where:

\[ R_{out} = Z_O / Z_L = \frac{1}{g_{ds1} + g_{dc2}} \]

In the analysis above, we used the N and P notation to distinguish the two-type of transistor used in the common source amplifier. In Figure 1(b), MN is M1 and MP is M2. The small signal dc voltage gain is translated to:

\[ A_v = \frac{v_o}{v_i} = -g_{mN} \left( R_{ON} // R_{OP} \right) \]

where:

\[ R_{ON} = 1 / (\lambda_N I_{DSQ}) \]
\[ R_{OP} = 1 / (\lambda_P I_{DSQ}) \]
\[ g_{mN} = \sqrt{2\beta_N I_{DSQ}} \]
\[ I_{DSQ} = I_N = I_P = (\beta_N / 2)(V_{bias} - V_{SS} - V_{TN})^2 \]

\[ \beta_N = K_N (W_N / L_N) = (40E - 6)(9.6E - 6)/4.4E - 6 = 87.3 \text{ uA/V}^2 \]
\[ I_{DSQ} = (\beta_N / 2)(V_{bias} - V_{SS} - V_{TN})^2 = (87.3E - 6/2)(0 - (-2.5) - 1)^2 = 98.21 \text{ uA} \]
\[ g_{mN} = \sqrt{2\beta_N I_{DSQ}} = \sqrt{2}(87.3E - 6)(98.21E - 6) = 130.95 \text{ umho} \]
\[ R_{ON} = 1 / (\lambda_N I_{DSQ}) = 1 / [(0.2)(98.21E - 6)] = 0.509M \]
\[ R_{OP} = 1 / (\lambda_P I_{DSQ}) = 1 / [(0.2)(98.21E - 6)] = 0.509M \]
\[ A_v = -g_{mN} (R_{ON} // R_{OP}) = -(130.95E - 6)(0.509M//0.509M) = -33.18 \]
The low frequency input resistance $R_{in} = \infty$, since the input is capacitive. The output resistance $R_{out} = (R_{ON}/R_{OP}) = .2545M$. These calculations agree well with PSpice simulation results of:

**** SMALL-SIGNAL CHARACTERISTICS

$V(2)/VIN = -3.500E+01$

INPUT RESISTANCE AT VIN = $1.000E+20$

OUTPUT RESISTANCE AT V(2) = $2.536E+05$

3. High Frequency Small Signal Equivalent Circuit

Figure 3 shows all the parasitic capacitances in the common source amplifier. Figure 4 shows the high frequency small signal equivalent circuit of the common source amplifier circuit. Comparing Figure 4(b) and 4(c) one obtains:
\[ V_1 = V_S = V_i = V_{gs1}; \ V_2 = V_o \]

The current equation is:

\[
I_1 = sC_{gs1} V_1 + sC_{gd1} (V_1 - V_2) = s(C_{gs1} + C_{gdl}) V_1 - sC_{gd1} V_2
\]

\[
I_2 = g_m V_1 + sC_{gd1} (V_2 - V_1) + (g_{ds1} + sC_o) V_2 = (g_m - sC_{gd1}) V_1 + [g_{ds1} + s(C_{gdl} + C_o)] V_2
\]

Figure 4. The high frequency equivalent circuit: (a) All the parasitic capacitances, (b) Combining capacitances, and (c) two-port representation. The corresponding Y-parameter matrix is:
The overall voltage gain is:

\[
A_V = \frac{V_2}{V_1} = -\frac{y_{21}}{y_{22} + Y_L} = -\frac{g_{m1} - sC_{gd1}}{g_{ds1} + s(C_{gd1} + C_o) + g_{ds2}} = -\frac{g_{m1} - sC_{gd1}}{(g_{ds1} + g_{ds2}) + s(C_{gd1} + C_o)}
\]

\[
= -\frac{g_{m1}}{g_{ds1} + g_{ds2}} \left( \frac{1 - s\frac{C_{gd1}}{C_{gd1} + C_o}}{1 + s\frac{C_{gd1} + C_o}{g_{ds1} + g_{ds2}}} \right) = -A_{V0} \left( 1 - \frac{s}{p_1} \right)
\]

where:

\[
A_{V0} = -g_{m1}R_{out}; R_{out} = \frac{1}{g_{ds1} + g_{ds2}}
\]

\[
z_1 = \frac{g_{m1}}{C_{gd1}}
\]

\[
p_1 = w_{BW} = -\frac{1}{R_{out}C_{out}}; C_{out} = C_{gd1} + C_o = C_{gd1} + C_{gd2} + C_{db1} + C_{db2} + C_L
\]

\[
w_{GBW} = A_{V0}w_{BW} = \left( -g_{m1}R_{out} \right) \left( -\frac{1}{R_{out}C_{out}} \right) = \frac{g_{m1}}{C_{out}}
\]

That is, the \(w_{GBW}\) is directly proportional to the transconductance of the driver transistor and inversely proportional to the total output capacitance. The Bode Plot is shown in Figure 5.
Figure 5. Approximate bode plot of common source amplifier.

Experiments on Common Source Amplifier Circuits

1. Pspice Simulation Using the Netlist of NMOS Inverter with PMOS Current Load Including $C_{gs}$ and $C_{gd}$ Transistor Parasitic Capacitances Only.

Figure 1(b) is simulated with PSpice. Its netlist file is shown below. No area and perimeter are supplied for the source and drain. That is, PSpice will only compute the $C_{gs}$ and $C_{gd}$ in the simulation. This will be verified using the small signal circuit including $C_{gs}$ and $C_{gd}$ only, discuss in section 3.

*PSpice file for NMOS Inverter with PMOS Current Load
*Filename="Lab3.cir"
VIN 1 0 DC 0VOLT AC 1V
VDD 3 0 DC 2.5VOLT
VSS 4 0 DC -2.5VOLT
VG 5 0 DC 0VOLT  
M1 2 1 4 4 MN W=9.6U L=5.4U  
M2 2 5 3 3 MP W=25.8U L=5.4U

.MODEL MN NMOS VTO=1 KP=40U  
+ GAMMA=1.0 LAMBDA=0.02 PHI=0.6  
+ TOX=0.05U LD=0.5U CJ=5E-4 CJSW=10E-10  
+ U0=550 MJ=0.5 MJSW=0.5 CGSO=0.4E-9 CGDO=0.4E-9  
.MODEL MP PMOS VTO=-1 KP=15U  
+ GAMMA=0.6 LAMBDA=0.02 PHI=0.6  
+ TOX=0.05U LD=0.5U CJ=5E-4 CJSW=10E-10  
+ U0=200 MJ=0.5 MJSW=0.5 CGSO=0.4E-9 CGDO=0.4E-9

*Analysis  
.DC VIN -2.5 2.5 0.05  
.TF V(2) VIN  
.AC DEC 100 1HZ 10GHZ  
.PROBE  
.END

The extracted parameters are:

\[
A_v = A_{v0} - 3 \quad f_{BW} = 44.218\text{M} \\
A_v = 0 \text{ db} \quad f_{GBW} = 1.6127\text{G} \\
PM = 75.826^\circ
\]

The Bode Plot is shown below:
2. Pspice Simulation Using the Netlist of NMOS Inverter with PMOS Current Load Including All Transistor Parasitic Capacitances.

This is achieved by supplying the area and perimeter of the source and drain in the Pspice netlist.

* PSpice file for NMOS Inverter with PMOS Current Load
* Filename="Lab31.cir"
VIN 1 0 DC 0VOLT AC 1V
VDD 3 0 DC 2.5VOLT
VSS 4 0 DC -2.5VOLT
VG 5 0 DC 0VOLT
M1 2 1 4 4 MN W=9.6U L=5.4U AD=40.32P AS=40.32P PD=27.6U PS=27.6U
M2 2 5 3 3 MP W=25.8U L=5.4U AD=108.36P AS=108.36P PD=60U PS=60U

.MODEL MN NMOS VTO=1 KP=40U
+ GAMMA=1.0 LAMBDA=0.02 PHI=0.6
+ TOX=0.05U LD=0.5U CJ=5E-4 CJSW=10E-10
+ U0=550 MJ=0.5 MJSW=0.5 CGSO=0.4E-9 CGDO=0.4E-9
.MODEL MP PMOS VTO=-1 KP=15U
+ GAMMA=0.6 LAMBDA=0.02 PHI=0.6
+ TOX=0.05U LD=0.5U CJ=5E-4 CJSW=10E-10
+ U0=200 MJ=0.5 MJSW=0.5 CGSO=0.4E-9 CGDO=0.4E-9
* Analysis
.DC VIN -2.5 2.5 0.05
The extracted parameters are:

\[ A_v = A_{v0} - 3 \quad f_{BW} = 6.6672 \text{M} \]
\[ A_v = 0 \text{ db} \quad f_{GBW} = 223.441 \text{M} \]

The Bode Plot is shown below:

---

**3. Pspice Simulation Using Small Signal Equivalent Circuit Including Cgs and Cgd Transistor Parasitic Capacitances Only.**

The following MATLAB m file has been written to calculate the parasitic capacitance for each transistor by specifying W, L, VBD, and VBS.

```matlab
function [CGS, CGD, CBD, CBS] = cap(W,L,VBD,VBS)
% Mfile must be save under /MATLAB directory
%SPICE PARAMETERS
TOX = 0.05; % 0.05U
COX = 0.69; % 0.69 fF/um^2 COX=(3.9eo/TOX)
CGSO = 0.4; % 0.4E-9 F/m=0.4fF/um
CGDO = 0.4; % 0.4E-9 F/m=0.4fF/um
CI = 0.5; % 5E-4 F/m^2=0.5fF/um^2
CJSW = 1; % 10E-10 F/m = 1fF/um
```
LD = 0.5 \% 0.5U
MJ = 0.5;
MJSW = 0.5;
PHI=0.6; \% 0.5 V
\%
SPICE PARAMETERS END
LEFF=L-2*LD;
LMIN = 4.2; \% 7*(.6)=4.2;4.5u actual measurement from LAB3 layout
CGC = COX \* W \* LEFF;
CGSOX = CGSO \* W;
CGDOX = CGDO \* W;
CGS = CGSOX + (2/3) \* CGC;
CGD = CGDOX;
AD = W \* LMIN;
PD = 2*(W + LMIN);
AS = W \* LMIN;
PS = 2*(W + LMIN);
CBDJ = CJ/(1 - VBD/PHI)^MJ;
CBDJSW = CJSW/(1 - VBD/PHI)^MJSW;
CBD = AD*CBDJ + PD*CBDJSW;
CBD = CBDO;
CBCJ = CJ;

CBC = CBCJ\*W*LEFF;
CBSJ = CJ/(1 - VBS/PHI)^MJ;
CBSJSW = CJSW/(1 - VBS/PHI)^MJSW;
CBSO = AS*CBSJ + PS*CBSJSW;
CBS = CBSO + (2/3)* CBC;
The following is a sample call using the circuit for lab3.

For the NMOS transistor,

[CGS, CGD, CBD, CBS] = cap (9.6, 5.4, -2.5, 0)
CGS = 23.2704  CGD = 3.8400  CBD = 21.0116  CBS = 61.8400

For the PMOS transistor,

[CGS, CGD, CBD, CBS] = cap (25.8, 5.4, -2.5, 0)
CGS = 62.5392  CGD = 10.3200  CBD = 50.2325  CBS = 152.0200

C_o = C_{DBn} + C_{DBp} + C_{DGp} = 21.0116 + 50.2325 + 10.32 = 81.5641 fF
CGSn = 23.2704 fF
CGDn = 3.8400 fF
* Small signal equivalent circuit of NMOS inverter with PMOS
* Current load. Only CGS CGD are calculated
* Filename=lab3eqn.cir"
Vin  0  AC 1V  
Rin  0  1E+20  
Cgd  1  2  3.84fF  
Cgs  1  0  23.27fF  
Gm  2  0  1  0  130.95u  
Ro  2  0  .2545Meg  
Co  2  0  10.32fF  
.TF  V(2)  Vin  
.AC  DEC  100  1HZ  10GHZ  
.PROBE  
.END  

The extracted parameters are:

\[ A_v = A_{v0} - 3 \quad f_{BW} = 42.341M \]

\[ A_v = 0 \text{ db} \quad f_{GBW} = 1.5493G \]

Comparing with theoretical calculation:

\[ w_{GBW} = \frac{g_m}{C_0} = \frac{130.95E-6}{10.32E-15} = 12.69x10^9 \]

\[ f_{GBW} = \frac{w_{GBW}}{2\pi} = \frac{12.69E9}{2\pi} = 2.02x10^9 = 2.02G \]

\[ w_{BW} = \frac{1}{R_o C_0} = \frac{1}{(.2545E6)(10.32E-15)} = 0.381x10^9 \]

\[ f_{BW} = \frac{w_{BW}}{2\pi} = \frac{0.38E9}{2\pi} = 60x10^6 = 60M \]

The Bode Plot is shown below:
4. Pspice Simulation Using Small Signal Equivalent Circuit
Including All Transistor Parasitic Capacitances.

* Small signal equivalent circuit of NMOS inverter with PMOS
* Current load.
* Filename = "lab3eq.cir"
Vin 1 0 AC 1V
Rin 1 0 1E+20
Cgd 1 2 3.84fF
Cgs 1 0 23.27fF
Gm 2 0 1 0 130.95u
Ro 2 0 .2545Meg
Co 2 0 81.5641fF
.TF V(2) Vin
.AC DEC 100 1HZ 10GHZ
.PROBE
.END

The extracted parameters are:

\[ A_V = A_{V0} - 3 \quad f_{BW} = 7.3485M \]
\[ A_V = 0 \text{ db} \quad f_{GBW} = 235.957M \]

Comparing with theoretical calculation:
The Bode Plot is shown below:

\[ w_{GBW} = \frac{g_m}{C_o} = \frac{130.95 \times 10^{-6}}{81.56 \times 10^{-15}} = 1.6054 \text{G} \]

\[ f_{GBW} = \frac{w_{GBW}}{2\pi} = \frac{1.6054 \times 10^9}{2\pi} = 256 \text{M} \]

\[ w_{BW} = \frac{1}{R_o C_o} = \frac{1}{(0.2545 \times 10^6)(81.56 \times 10^{-15})} = 0.048 \text{G} \]

\[ f_{BW} = \frac{w_{BW}}{2\pi} = \frac{0.048 \times 10^9}{2\pi} = 7.64 \text{M} \]

The Bode Plot is shown below:

---

**Common Source Amplifier Design Procedure**

**Design Specification**

Design a common source amplifier with a gain of \( A_v = 50 \) and output impedance of \( R_o = 1 \text{Meg} \).

\[ R_o = R_{ON}/R_{OP} \]

Assume \( R_{ON} = R_{OP} \), hence

\[ R_{ON} = R_{OP} = 2R_o = 2 \text{Meg} \]
\[
R_{\text{ON}} = \frac{1}{\lambda_n I_{\text{DSQ}}} = R_{\text{OP}} = \frac{1}{\lambda_p I_{\text{DSQ}}}
\]

Solving for \( I_{\text{DSQ}} \),
\[
I_{\text{DSQ}} = \frac{1}{\lambda_n R_{\text{ON}}} = \frac{1}{\lambda_p R_{\text{OP}}} = \frac{1}{(0.02)(2E6)} = 25uA
\]

From the gain equation the \((W/L)\), can be obtained as follows:
\[
A_v = -g_{mn}R_O = -\sqrt{2\beta_n I_{\text{DSQ}}}R_O = -\sqrt{2K_N(W_N/L_{\text{Neff}})I_{\text{DSQ}}}R_O
\]
\[
(W_N/L_{\text{Neff}}) = \frac{(A_v/R_O)^2}{2K_NI_{\text{DSQ}}} = \frac{(50/1E6)^2}{2(40E-6)(25E-6)} = 5/4
\]

Using technology with \( \lambda = 0.6u \), the \( W, L \) are selected as follows:
\[
W_N = 5\lambda = 5(0.6) = 3u
\]
\[
L_{\text{Neff}} = 4\lambda = 4(0.6) = 2.4u
\]
\[
L_N = L_{\text{Neff}} + 2LD = 2.4u + 2(0.5u) = 3.4u
\]

The drawn length must be multiple of \( \lambda \), hence \( L_N = 3.6u \) (\( = 6\lambda \)), the nearest computed value must be selected.

The \( W, L \) of the PMOS are computed to achieve \( \beta_R = 1 \), that is
\[
\beta_R = \frac{K_p(W_p/L_p)}{K_N(W_N/L_{\text{Neff}})} = \frac{K_p W_p}{K_N W_N} = 1 \text{; since } L_{\text{Neff}} = L_p
\]
\[
W_p = \frac{K_N W_N}{K_p} = \frac{(40E-6)(3u)}{(15E-6)} = 8u; \text{ select } 7.8u \text{ (}=13\lambda)
\]
\[
L_p = L_N = 3.6u
\]
Figure 1. Common source amplifier using current mirror to establish the bias current.

The common source amplifier is initially simulated using Pspice with $V_{bias}$ set to 0 to obtain the DC transfer characteristic. The actual $V_{bias}$ is then located at the center of the transition region, region 3 of DC transfer characteristic.

*PSpice file for NMOS Inverter with PMOS Current Load
*Filename="Lab3tst.cir"
VIN 1 0 DC 0VOLT AC 1V
VDD 3 0 DC 2.5VOLT
VSS 4 0 DC -2.5VOLT
M1 2 1 4 4 MN W=3U L=3.6U
M2 2 5 3 3 MP W=7.8U L=3.6U
M3 5 5 3 3 MP W=7.8U L=3.6U
IB 5 4 25U

.MODEL MN NMOS VTO=1 KP=40U
+ GAMMA=1.0 LAMBDA=0.02 PHI=0.6
+ TOX=0.05U LD=0.5U CJ=5E-4 CJSW=10E-10
+ U0=550 MJ=0.5 MJSW=0.5 CGSO=0.4E-9 CGDO=0.4E-9
.MODEL MP PMOS VTO=-1 KP=15U
+ GAMMA=0.6 LAMBDA=0.02 PHI=0.6
+ TOX=0.05U LD=0.5U CJ=5E-4 CJSW=10E-10
+ U0=200 MJ=0.5 MJSW=0.5 CGSO=0.4E-9 CGDO=0.4E-9
*Analysis
The simulation results are for \( V_{\text{bias}} = 0 \). Hence the following small signal characteristics are not what we are looking for.

**** SMALL-SIGNAL CHARACTERISTICS

\[
\frac{V(2)}{V_{\text{IN}}} = -4.066 \times 10^{-01}
\]

INPUT RESISTANCE AT \( V_{\text{IN}} \) = 1.000E+20

OUTPUT RESISTANCE AT \( V(2) \) = 1.986E+04

The above simulation results will give us the node voltage \( V_5 = V_G \).

<table>
<thead>
<tr>
<th>NODE</th>
<th>VOLTAGE</th>
<th>NODE</th>
<th>VOLTAGE</th>
<th>NODE</th>
<th>VOLTAGE</th>
<th>NODE</th>
<th>VOLTAGE</th>
</tr>
</thead>
<tbody>
<tr>
<td>( 1)</td>
<td>0.0000</td>
<td>( 2)</td>
<td>-2.0602</td>
<td>( 3)</td>
<td>2.5000</td>
<td>( 4)</td>
<td>-2.5000</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( 5)</td>
<td>.4667</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

With node voltage \( V_G \) known, the approximate \( V_{\text{bias}} \) can be calculated as follows:

\[
V_{\text{bias}} = V_{SS} + V_{TN} + (V_{DD} - V_G + V_{TP})/\sqrt{\beta} = -2.5 + 1 + (2.5 - V_G - 1)/\sqrt{I} = -V_G
\]

\( V_{\text{bias}} = -V_5 = -V_G = -.4667 \)

The node voltage \( V_G \) can also be calculated theoretically, this will be shown in the next section.

To obtain the desired small signal characteristics, the \( V_{\text{bias}} \) must be set correctly by changing one line in the Pspice netlist.

\textbf{VIN 1 0 DC \(-0.4667\) VOLT AC 1V}

The small signal characteristics show that the design specifications are achieved within 5%: \( A_v = -50.8 \), \( R_o = 1.027 \text{Meg} \).

**** SMALL-SIGNAL CHARACTERISTICS
\[ V(2)/V_{\text{IN}} = -5.080E+01 \]

**INPUT RESISTANCE AT VIN = 1.000E+20**

**OUTPUT RESISTANCE AT V(2) = 1.027E+06**

<table>
<thead>
<tr>
<th>NODE VOLTAGE</th>
<th>NODE VOLTAGE</th>
<th>NODE VOLTAGE</th>
<th>NODE VOLTAGE</th>
</tr>
</thead>
<tbody>
<tr>
<td>(1) -0.4667</td>
<td>(2) -0.6650</td>
<td>(3) 2.5000</td>
<td>(4) -2.5000</td>
</tr>
<tr>
<td>(5) 0.4667</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Increasing The Gain of Common Source Amplifier**

The new specification is to increased the gain to \( Av = 70 \), and maintaining \( R_o = 1 \text{Meg} \).

Using the current mirror principle the \( I_{DSQ} = 25 \text{uA} = I_{\text{bias}} \) can be maintained by passing \( I_{\text{bias}} \) to M3. With a constant \( I_{DSQ} \), \( R_o \) will also be constant. The new gain can be achieved as follows:

\[
\frac{A_{V2}}{A_{V1}} = -\frac{g_{m2}}{g_{m1}} = \sqrt{\frac{2K_N (W_{N2}/L_{\text{Neff}})I_{DSQ}}{2K_N (W_{N1}/L_{\text{Neff}})I_{DSQ}}} = \sqrt{\frac{W_{N2}}{W_{N1}}}
\]

\[
W_{N2} = \left(\frac{A_{V2}}{A_{V1}}\right)^2 W_{N1} = \left(\frac{70}{50}\right)^2 3u = \frac{49}{25} 3u \approx 6u
\]

**Theoretical Calculation of \( V_G \)**

PMOS transistor is in saturation whenever,

\[
|V_{\text{GSP}}| - |V_{\text{TP}}| < |V_{\text{DSP}}|
\]  --(1)

For PMOS transistor M3, the drain is connected to gate, hence eq (1) is always satisfied. M3 is always operating in saturation mode. Hence, the drain current is given by:

\[
I_{\text{bias}} = I_{P3} = (\beta_p/2)(|V_G - V_{\text{DD}}| - |V_{\text{TP}}|)^2 = (\beta_p/2)(1.5 - V_G)^2
\]  --(2)

Solving for \( V_G \),
\[
V_G = 1.5 - \frac{2I_{\text{bias}}}{\beta_p} = 1.5 - \frac{2I_{\text{bias}}}{K_p(W_p/L_{\text{eff}})} = 1.5 - \frac{2(25E-6)}{15E-6(7.8/2.6)} = 0.4459
\]

Simulation result is 0.4667

Changing the W/L of M1 to increase the gain will alter the \( \beta_R \) ratio.

\[
\beta_R = \frac{K_N(W_N/L_{Neff})}{K_p(W_p/L_{Peff})} = \frac{K_N W_N}{K_p W_p} = \frac{(40E-6)(6E-6)}{(15E-6)(7.8E-6)} = 2.05
\]

The new theoretical \( V_{\text{bias}} \) is calculated,

\[
V_{\text{bias}} = V_{SS} + V_{TN} + (V_{DD} - V_G + V_{TP})/\sqrt{\beta_R} = -2.5 + 1 + (2.5 - 0.4459 - 1)/\sqrt{2.05} = -0.764
\]

Again the actual \( V_{\text{bias}} \) is determined from the DC transfer characteristics, \( V_{\text{bias}} = -0.777 \) which is very close to the theoretical calculation above.

The new circuit is simulated by changing the following two lines in the Pspice netlist:

\[
\begin{align*}
\text{VIN} & \ 1 \ 0 \ \text{DC} -0.777 \text{VOLT AC} \ 1 \text{V} \\
\text{M1} & \ 2 \ 1 \ 4 \ 4 \ \text{MN} \ W=6U \ L=3.6U
\end{align*}
\]

The simulation results show that the desired small signal characteristics are within 5%, \( A_v = -72.61 \), and \( R_o = 1.038 \text{Meg} \)

**** SMALL-SIGNAL CHARACTERISTICS

\[
\begin{align*}
V(2)/\text{VIN} & = -7.261E+01 \\
\text{INPUT RESISTANCE AT VIN} & = 1.000E+20 \\
\text{OUTPUT RESISTANCE AT V(2)} & = 1.038E+06
\end{align*}
\]

NODE VOLTAGE

\begin{align*}
\begin{array}{cccc}
\text{NODE} & \text{VOLTAGE} \\
1 & -0.7770 \\
2 & -0.1122 \\
3 & 2.5000 \\
4 & -2.5000 \\
5 & 0.4667 \\
\end{array}
\end{align*}
Replace the current source by resistor R

![Circuit Diagram]

Figure 2. Replacing IB by R

In Figure 2,

\[
I_{\text{bias}} = \frac{V_G - V_{SS}}{R} = \frac{V_G + 2.5}{R} = \frac{V_G + 2.5}{I_{\text{bias}}} = \frac{0.4667 + 2.5}{25E-6} = 0.119\text{Meg} \approx 120k
\]

To simulate the new circuit, the Pspice netlist is modified as follows:

IB 5 4 25U (Delete this line)

R 5 4 120k (Add this line)

Simulation results are very closed with the circuit with current source.

**** SMALL-SIGNAL CHARACTERISTICS
V(2)/VIN = -7.261E+01
INPUT RESISTANCE AT VIN = 1.000E+20
OUTPUT RESISTANCE AT V(2) = 1.043E+06

<table>
<thead>
<tr>
<th>NODE VOLTAGE</th>
<th>NODE VOLTAGE</th>
<th>NODE VOLTAGE</th>
<th>NODE VOLTAGE</th>
<th>NODE VOLTAGE</th>
</tr>
</thead>
<tbody>
<tr>
<td>( 1) -.7770</td>
<td>( 2) -.3597</td>
<td>( 3) 2.5000</td>
<td>( 4) -2.5000</td>
<td></td>
</tr>
<tr>
<td>( 5) .4716</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**The Effect of Eliminating Parasitic Capacitance Parameters**

Eliminate terms in the MODEL that refers to parasitic capacitances. The new Pspice netlist is shown below. The simulation results show that the bandwidth of amplifier becomes infinite.

*PSpice file for NMOS Inverter with PMOS Current Load
*Filename="Lab3tst1.cir"
VIN 1 0 DC -0.777VOLT AC 1V
VDD 3 0 DC 2.5VOLT
VSS 4 0 DC -2.5VOLT

M1 2 1 4 4 MN W=6U L=3.6U
M2 2 5 3 3 MP W=7.8U L=3.6U
M3 5 5 3 3 MP W=7.8U L=3.6U
R 5 4 120k
*IB 5 4 25U

.MODEL MN NMOS VTO=1 KP=40U
+ GAMMA=1.0 LAMBDA=0.02 PHI=0.6
+ TOX=0.05U LD=0.5U
.MODEL MP PMOS VTO=-1 KP=15U
+ GAMMA=0.6 LAMBDA=0.02 PHI=0.6
+ TOX=0.05U LD=0.5U
*Analysis
.DC VIN -2.5 2.5 0.05
.TF V(2) VIN
.AC DEC 100 1HZ 1000GHZ
.PROBE
.END