Lab 4: IC Extraction and Post Layout Simulation

This Lab will go over:

1. Circuit Extraction.
2. Layout versus Schematic (LVS).
3. Post Extraction Simulation.

1. Circuit Extraction

Now that your circuit is laid out with no DRC errors, it is time to check if it is an electrical equivalent of your nand2 schematic.

Execute (VLE) Verify>Extract… A pop-up like Figure 1 should appear.

![Extractor](image)

Figure 1. Running the extractor.
Click on the set switches button in the extractor pop-up and a list of choice should appear like in Figure 2.

Figure 2: Selecting Extract parasitic capacitances.

Click on Extract_parasitic_caps and press **OK**.

Your extractor pop-up should look like Figure 3.
Figure 3: Extractor all set to go.

Click **OK** to run the extractor. The **CIW** should give no errors like in Figure 4.

Figure 4: Extracted nand2 with no errors.
2. Layout versus Schematic (LVS)

An LVS check makes sure that the circuit you laid out is equivalent to the one you entered into your schematic. To run an LVS check, execute (VLE)Verify>LVS…. A pop-up should appear like Figure 5.

Use the Browse button to select which schematic and which extracted view you are going to check for equivalence. The pop-up should be filled out just like Figure 5. Click Run to start. This will take several minutes. When the LVS check is successful a pop-up like Figure 6 should appear.

![Figure 5: Running an LVS Check](image-url)
Figure 6: Successful completion of an LVS check.

LVS successful do not necessarily mean that the two circuits match. You must check the LVS output by clicking the **Output** button in the LVS pop-up. The display should indicate that the net-lists match.
To see what your extracted nand2 looks like go back to the library manager and select the extracted view of your nand2. Your extracted view should look like Figure 8. It is a combination of a layout and schematic. You will see four transistors and parasitic capacitors. These capacitors
could affect the performance of your circuit so you will need to re-run your simulation to verify that it still meets specification.

Figure 8: Extracted view of the nand2.
3. Post Extraction Simulation

In post extraction simulation, you verify that your circuit still meets your specification with the additions of parasitic capacitances. For example, in a schematic two wires that are not connected there is no transfer of AC voltage or current. In a layout where two metal lines are close, but not connected there is a capacitance between the two that will cause cross talk. Post extraction simulation will show these errors.

To perform a post extraction simulation on your nand2 gate:

1. Open up your nand2_TB schematic.
2. Start the Affirma Analog environment.
3. Set up the simulation as in Figure 9.

![Figure 9: Setting for post extraction simulation.](image)

Execute (ADE L)Setup>Environment…. A pop-up like Figure 10 should appear.

In the Switch View List insert the view extracted before the spectreS view like in Figure 10. Click OK.

Now run the simulation. Your results should match Figure 11.
Note: If you want to use the schematic view for simulation you have to delete the extracted view from the switch list.

![Environment Options](image)

Figure 10: Inserting the extracted view.
Figure 11: The extracted simulation.
The delay is practically the same as with schematic view. If the circuit met the specification, you would be done. If not, you would have to alter the widths of the transistors or modify the layout, do DRC, Extract, and re-simulate until it did.

**Assignment:**

Perform post layout simulation for your inverter.