Electronic Integration for Smart Sensors

A general smart sensor system block diagram is a closed-loop system consisting of five blocks: Sensor, Signal Processing, AD, Digital Decision Logic, and DA.

![Smart Sensor System Block Diagram](image)

The igert students, over the past several years, have been learning the expertise in creating and developing each block. These are described in the following sections:

**Sensor**

There are different varieties of sensors that are being developed and studied by igert students. The sense signal can be due to change in resistance, capacitance, or frequency. Each of these sensors requires different detecting circuits. But the subsequent processing blocks are common to any sensors, as shown in Figure 1.

**Signal Processing**

In any sensor applications, the first thing to be done is to enhance the quality of the detected signal. One such enhancement is to improve the signal to noise ratio by filtering. In many sensor applications, we have pre-knowledge about the operating frequency range of the sensor signal. The noise are usually of wide-spectrum, by only allowing the sensor signal over its operating range using band-pass filtering will increase the signal to noise ratio. In biological application, the desired sensor signal is usually superimposed with the periodic heart bit signal. This periodic signal can be eliminated using band-reject filter. The igert students learned how to create a continuous time universal second order filters. The benefits of the continuous time filters are the elimination of noise introduce by switching in digital filters. This filter is called universal, because the same filters becomes low-pass, high-pass, band-pass, or band-
reject filter by simply changing the external connections. A typical universal second order filter schematic and response curves are shown in Figures 2, and 3. In addition, igert students learned how to develop a higher order filters using butterworth and chebyshev transfer functions for more demanding applications. Also, signal amplification is usually required to build-up the signal level to the required input dynamic range (typically 0 to 5V) of the analog-to-digital converter (AD). This is achieved by providing igert students with the knowledge of designing operational amplifier to achieve any design specifications.

Figure 2. Universal Second Order Filter Schematic Diagram.
Figure 3 (a). Low-pass filter response curve.

Figure 3(b). High-pass filter response curve.
To exploit the digital decision logic to create smart sensors, an analog to digital converter is necessary. For complete integration, we need to be able to create our own AD converter. The design should be high-speed, and can be of any size or precision to accommodate a wide-range of applications. We have developed such an AD converter.
based on neural network architecture that achieves a successive approximation type AD asynchronously. The maximum speed of the AD is equal to $n^* \Delta t$, where $n$ is the number of bits and $\Delta t$ is the propagation delay of the comparator. This design was successfully implemented using wide-swing high-speed comparator, and using the technology with high-res layer. This the first time, we were able to successfully build an 8-bit AD due to the requirements that we need to use a very high resistance value to reduce the loading effects on the comparators. Figure 4 shows the schematic diagram of the 4-bit AD. Figure 5 shows the entire layout within the padframe. In the past, this AD architecture will practically filled-up the entire silicon area even for 4-bit AD. Figure 6 shows the simulation results of the 4-bit AD.

Figure 4. 4-bit AD R-2R Architecture Schematic Diagram.
Figure 5. The 4-bit AD layout within the padframe.
Figure 6. 4-bit AD Simulation Results.

**Digital Decision Logic**

Decision making to create a family of smart sensors is best delegated to the digital world, where hosts of digital devices can be used such as FPGA, micro-controller, microprocessor, and custom VLSI. Igert students learn how to create custom VLSI by writing VHDL code that describes the desired decision logic to be implemented. The code is then simulated, synthesized, and layout using CADENCE tools. This custom VLSI can then integrated with the rest of the analog circuits by proper power supply isolation to eliminate the propagation of digital switching noise.

**DA – Digital to Analog**

A high speed digital to current converter has been developed that can operate up to 50MHz. It is based on precise metering of current sources. In an 8-bit design, there are 256 identical current sources each can source 10uA. Each current source has a decoding circuit that determines whether it will be selected to contribute to the total current. The decoding circuit was designed based on thermometer decoding of the binary number. Table 1 shows the thermometer decoding of 4-bit binary number. That is, the binary...
The 8-bit binary input is split into two groups of 4-bit number. The upper 4-bit is used to select the sixteen columns of current sources after thermometer decoding. The lower 4-bit is used to select the sixteen rows of current sources after binary decoding.
Figure 7. Current Source Decoding Logic.

Figure 7 shows the current source decoding logic. The decoding logic has three inputs; the current source is selected according to

\[
\text{OUT} = \text{ROW}_{N-1} \text{ AND (ROW}_N \text{ OR COL}_N)
\]

That is, the current source will be selected or source in the OUT terminal when the previous row (ROW\(_{N-1}\)) is on and either the current row (ROW\(_N\)) or current column (COL\(_N\)) is on. The architecture of the 8-bit DA is shown in Figure 8. Each square block represents a current source with the decoding logic circuit. Each row has two inputs corresponding to previous row (ROW\(_{N-1}\)) and current row (ROW\(_N\)). Each column has one input, current column (COL\(_N\)). In addition, the following boundary conditions are needed:

ROW\(_0\) = 1, ROW\(_{16}\) = 0, and COL\(_{16}\) = 0

Figure 8. 8-bit DA Symbolic Block Diagram.
To explain its operation, let us say the binary input \((00110011)_2 = 48_{10}\). We want to show that 48 current sources will be turned on or selected. After thermometer decoding the following rows and columns will be on:

\[
\begin{align*}
\text{ROW}_1 &= \text{ROW}_2 = \text{ROW}_3 = 1 \\
\text{COL}_1 &= \text{COL}_2 = \text{COL}_3 = 1
\end{align*}
\]

For row 1, \(N=1\)
\[
\text{OUT} = (\text{ROW}_0 = 1) \text{ AND } ((\text{ROW}_1 = 1) \text{ OR } \text{COL}_X = X) = 1
\]
That is, the entire row 1 is on regardless of the value of each column.

For row 2, \(N=2\)
\[
\text{OUT} = (\text{ROW}_1 = 1) \text{ AND } ((\text{ROW}_2 = 1) \text{ OR } \text{COL}_X = X) = 1
\]
That is, the entire row 2 is on regardless of the value of each column.

For row 3, \(N=3\)
\[
\text{OUT} = (\text{ROW}_2 = 1) \text{ AND } ((\text{ROW}_3 = 1) \text{ OR } \text{COL}_X = X) = 1
\]
That is, the entire row 3 is on regardless of the value of each column.

For row 4, \(N=4\)
\[
\text{OUT} = (\text{ROW}_3 = 1) \text{ AND } ((\text{ROW}_4 = 0) \text{ OR } \text{COL}_X = 1) = 1
\]
That is, in row 4 only cols 1, 2, 3 will be on.

For row \(>4\), \(N>=5\)
\[
\text{OUT} = (\text{ROW}_{N-1} = 0) \text{ AND } ((\text{ROW}_N = 0) \text{ OR } \text{COL}_X = 1) = 1
\]
That is, the entire row is off for \(N>=5\).

Figure 8 shows that precisely 48 current sources are shaded or selected.

If in some application voltage output is required, you only need to connect the current output to a load resistor.