CMOS Inverter Amplifier

Figure 1. CMOS inverter amplifier circuit

1. Low Frequency Small Signal Equivalent Circuit

Figure 2(a) shows its low frequency equivalent circuit. That is, all the stray capacitances are ignored. In this circuit, PMOS transistor MP acts as the load of the driver NMOS transistor MN, and vice versa. That is, each transistor acts as the load of the other. Hence, an unloaded two-port parameters are to be determined. Comparing Figure 2(a) and Figure 2(b), one obtains:

\[ Y_L = 0 \text{ (or } Z_L = \infty); \quad Y_S = \infty \text{ (or } Z_S = 0) \]

\[ V_1 = V_i = V_{gs1} \]

and

\[ V_2 = V_o \]

From Fig 2, the current equations are derived to obtain the Y parameters:

\[ I_1 = 0 \]

\[ I_2 = (g_{m1} + g_{m2})V_1 + (g_{ds1} + g_{ds2})V_2 \]
Figure 2. CMOS inverter low frequency equivalent circuit

That is, the $Y$-parameter matrix is given by:

$$Y = \begin{bmatrix} 0 & 0 \\ g_{m1} + g_{m2} & g_{ds1} + g_{ds2} \end{bmatrix}; \det Y = 0$$

The input impedance of common source circuit,

$$Z_i = \frac{Y_{22} + Y_L}{\det Y + y_{11}Y_L} = \frac{g_{ds1} + g_{ds2} + 0}{0 + (0)(0)} = \infty$$

The output impedance of the common source circuit,

$$Z_o = \frac{y_{11} + Y_s}{\det Y + y_{22}Y_s} = \frac{1}{y_{22}} = \frac{1}{g_{ds1} + g_{ds2}}$$

The dc voltage gain is,

$$A_{V_0} = -\frac{y_{21}}{y_{22} + Y_L} = -\frac{g_{m1} + g_{m2}}{g_{ds1} + g_{ds2}} \text{ or }$$

$$A_{V_0} = -2g_{m1}Z_o = -g_{m1}R_{out}; \ R_{out} = Z_o = \frac{1}{g_{ds1} + g_{ds2}}; g_{m1} = g_{m2}$$
The current gain is,
\[ A_1 = -\frac{\frac{y_{21}}{y_{11}} Y_L}{\text{det}Y + \frac{y_{11}}{y_{11}} Y_L} = \frac{(g_{m1} + g_{m2})(0)}{0 + 0(0)} = \text{undefined} \]

The small signal dc gain can also be derived mathematically. This elegant method is applicable to this circuit configuration only.

\[ I_N = I_p \]
\[ I_{DSN}(V_i, V_o) = -I_{DSP}(V_i, V_o) \]
\[ dI_{DSN}(V_i, V_o) = -dI_{DSP}(V_i, V_o) \]

\[ \frac{\partial I_{DSN}}{\partial V_i} dV_i + \frac{\partial I_{DSP}}{\partial V_o} dV_o = -\left(\frac{\partial I_{DSN}}{\partial V_i} dV_i + \frac{\partial I_{DSP}}{\partial V_o} dV_o\right) \]

Solve for \( A_v = \frac{dV_i}{dV_o} \)

\[ A_v = dV_i / dV_o = \left[-(\frac{\partial I_{DSN}}{\partial V_i} - \frac{\partial I_{DSP}}{\partial V_o})\right] / \left(\frac{\partial I_{DSN}}{\partial V_i} + \frac{\partial I_{DSP}}{\partial V_o}\right) \]

For the MN transistor:
\[ V_{GSN} = V_i - V_{SS}, \quad V_{DSN} = V_o - V_{SS}. \]
Therefore \( \partial V_i = \partial V_{GSN} \), and \( \partial V_o = \partial V_{DSN} \)

For the MP transistor:
\[ V_{GSP} = V_i - V_{DD}, \quad V_{DSP} = V_o - V_{DD}. \]
Therefore \( \partial V_i = \partial V_{GSP} \), and \( \partial V_o = \partial V_{DSP} \)

That is, the gain equation is rewritten as follows:

\[ A_v = \frac{dV_i}{dV_o} = \left[-(\frac{\partial I_{DSN}}{\partial V_i} - \frac{\partial I_{DSP}}{\partial V_o})\right] / \left(\frac{\partial I_{DSN}}{\partial V_i} + \frac{\partial I_{DSP}}{\partial V_o}\right) \]

\[ A_v = -\left[g_{mN} + g_{mP}\right] / \left[g_{DSN} + g_{DSP}\right] \]

Hence the equivalent circuit of the inverter is given in Figure 1(b).

2. CMOS Inverter Static Characteristic

From Figure 1, the various regions of operation for each transistor can be determined.

**MN Transistor Operating Regions:**
- **Cutoff**
  \[ V_{GSN} < V_{TN} \]
  \[ V_i - V_{SS} < V_{TN} \]
  \[ V_i < V_{TN} + V_{SS} = 1+(-2.5)=-1.5 \]
  \[ V_i < -1.5 \]
- **Saturation**
  \[ V_{GSN} - V_{TN} < V_{DSN} \]
  \[ V_i - V_{SS} - V_{TN} < V_o - V_{SS} \]
  \[ V_i - 1 < V_o \]
- **Ohmic**
  \[ V_i - 1 >= V_o \]

**MP Transistor Operating Regions:**
- **Cutoff**
  \[ |V_{GSP}| < |V_{TP}| \]
  \[ |V_i - V_{DD}| < |V_{TP}| \]
\[ V_{DD} - V_i < - V_{TP} \; \text{since} \; V_{TP} < 0 \]

\[ V_{TP} + V_{DD} = (-1) + 2.5 = 1.5 \text{V} \]

\[ V_i > 1.5 \text{V} \]

- **Saturation**
  \[
  [V_{GSP}] - |V_{TP}| < |V_{DSP}|
  \]
  \[
  |V_i - V_{DD}| - |V_{TP}| < |V_o - V_{DD}|
  \]

- **Ohmic**
  \[ V_i + 1 \leq V_o \]

These are summarized as follows:

<table>
<thead>
<tr>
<th>Operating Region</th>
<th>MN</th>
<th>MP</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cutoff</td>
<td>( V_i &lt; -1.5 \text{V} )</td>
<td>( V_i &gt; 1.5 \text{V} )</td>
</tr>
<tr>
<td>Saturation</td>
<td>( V_i - 1 &lt; V_o )</td>
<td>( V_i + 1 &gt; V_o )</td>
</tr>
<tr>
<td>Ohmic</td>
<td>( V_i - 1 \geq V_o )</td>
<td>( V_i + 1 \leq V_o )</td>
</tr>
</tbody>
</table>

The various regions of operating of inverting CMOS amplifier are summarized as follows:

<table>
<thead>
<tr>
<th>Operating Region</th>
<th>MN</th>
<th>MP</th>
</tr>
</thead>
<tbody>
<tr>
<td>Region I</td>
<td>Cutoff</td>
<td>Ohmic</td>
</tr>
<tr>
<td>Region II</td>
<td>Saturation</td>
<td>Ohmic</td>
</tr>
<tr>
<td>Region III</td>
<td>Saturation</td>
<td>Saturation</td>
</tr>
<tr>
<td>Region IV</td>
<td>Ohmic</td>
<td>Saturation</td>
</tr>
<tr>
<td>Region V</td>
<td>Ohmic</td>
<td>Cutoff</td>
</tr>
</tbody>
</table>

These regions are shown in the Pspice transfer characteristic graph, see Figure 3.

With zero output current (assuming driving a CMOS type load) the load current is equal to the

\[ i_P = i_N \]

For the PMOS transistor MP, the current equation for saturated case is given by:

\[ i_{DS} = -i_s = -\left(\beta / 2\right)\left[V_{DS} - V_T\right]^2 \text{ when } [V_{DS} - V_T] \leq [V_{DS}] \]

\[ i_P = \left(\beta / 2\right)\left[V_i - V_{DD}\right]^2 \text{ when } [V_i - V_{DD}] \leq [V_P] \leq |V_o - V_{DD}| \]

The absolute value symbol can be eliminated by accounting for the sign of each term within the symbol.

For PMOS transistor the following hold: \( V_i < V_{DD}, V_{TP} < 0, V_o < V_{DD} < 0 \). The above current equations reduce to:

\[ i_P = \left(\beta / 2\right)(V_{DD} - V_o)^2 \text{ when } (V_{DD} - V_i) + V_{TP} \leq V_{DD} - V_o \text{ or } V_i - V_{TP} > V_o \]

Similarly, the PMOS current equation for the non-saturated case is given by:

\[ i_s = \frac{\beta}{2}(V_{DD} - V_i) + V_{TP} \text{ when } V_i - V_{TP} \leq V_o \]

For the NMOS driver transistor MN current equations are given by:

\[ i_N = \left(\beta / 2\right)(V_i - V_{SS} - V_{TN})^2 \text{ when } V_i - V_{SS} - V_{TN} \leq V_o - V_{SS} \text{ or } V_i - V_{TN} \leq V_o, \text{ TD is saturated.} \]

\[ i_N = \frac{\beta}{2}(V_i - V_{SS} - V_{TN})(V_o - V_{SS}) - (V_o - V_{SS})^2 / 2 \text{ when } V_i - V_{TN} > V_o, \text{ TD is non-saturated.} \]

**Inverter Static Characteristic**
The static characteristic is determined by equating the corresponding current equations at each voltage range:

1. \( V_i - V_{SS} < V_{TN} \), and \( V_i - V_{TP} < V_o \). The driver transistor MN is off, and MP is ohmic, hence \( V_o = V_{dd} \).

2. \( V_i - V_{SS} > V_{TN} \), \( V_i - V_{TN} < V_o \), and \( V_i - V_{TP} < V_o \). The transistor MN is saturated, and the transistor MP is ohmic.

\[
\left( \frac{\beta_n}{2} \right) (V_i - V_{SS} - V_{TN})^2 = \beta_p \left[ (V_{DD} - V_i + V_{TP}) (V_{DD} - V_O) - (V_{DD} - V_O)^2 / 2 \right]
\]

Solving for \( V_o \),

\[
V_o = (V_i - V_{TP}) + \sqrt{(V_{DD} - V_i + V_{TP})^2 - \beta_R (V_i - V_{SS} - V_{TN})^2} \text{ where } \beta_n = \frac{\beta_n}{\beta_p}
\]

3. \( V_i - V_{SS} > V_{TN} \), \( V_i - V_{TN} < V_o \), and \( V_i - V_{TP} > V_o \). The transistor MN is saturated, and the transistor MP is also saturated.

\[
\left( \frac{\beta_n}{2} \right) (V_i - V_{SS} - V_{TN})^2 = \left( \frac{\beta_p}{2} \right) (V_{DD} - V_i + V_{TP})^2
\]

This equation is independent of \( V_o \), it is used to determine the operating point \( V_{bias} \) of the inverter. This corresponds to the input voltage \( V_i \) when the output voltage \( V_o = (V_{DD} + V_{SS}) / 2 = (2.5 + 2.5) / 2 = 0 \).

Solving for \( V_{bias} \),

\[
V_i = V_{bias} = \frac{V_{DD} + V_{TP} + \sqrt{\beta_R (V_{SS} + V_{TN})}}{1 + \sqrt{\beta_R}}
\]

4. \( V_i - V_{SS} > V_{TN} \), \( V_i - V_{TN} > V_{O} \), and \( V_i - V_{TP} > V_{O} \). The transistor MN is ohmic, and the transistor MP is saturated.

\[
\beta_n = [ (V_i - V_{SS} - V_{TN}) (V_O - V_{SS}) - (V_O - V_{SS})^2 / 2 ] = \left( \frac{\beta_p}{2} \right) (V_{DD} - V_i + V_{TP})^2
\]

Solving for \( V_o \),

\[
V_o = (V_i - V_{TN}) - \sqrt{(V_i - V_{SS} - V_{TN})^2 - (V_{DD} - V_i + V_{TP})^2 / \beta_R}
\]

5. \( V_i - V_{TN} > V_{O} \), and \( V_i - V_{DD} > V_{TP} \). The transistor MN is ohmic, and MP is off. Hence \( V_o = V_{SS} \).

*Pspice file for CMOS Inverter
*Filename="cmos.cir"
VIN 1 0 DC 0V AC 1VOLT
VDD 3 0 DC 2.5VOLT
VSS 4 0 DC -2.5VOLT
M1 2 1 4 4 NMOS1 W=9.6U L=5.4U
M2 2 1 3 3 PMOS1 W=25.8U L=5.4U
.Model NMOS1 NMOS VTO=1.0 KP=40U
+ GAMMA=1.0 LAMBDA=0.02 PHI=0.6
+ TOX=0.05U LD=0.5U CJ=5E-4 CJSW=10E-10
+ U0=550 MJ=0.5 MJSW=0.5 CGSO=0.4E-9 CGDO=0.4E-9
.Model PMOS1 PMOS VTO=-1.0 KP=15U
+ GAMMA=0.6 LAMBDA=0.02 PHI=0.6
+ TOX=0.05U LD=0.5U CJ=5E-4 CJSW=10E-10
+ U0=200 MJ=0.5 MJSW=0.5 CGSO=0.4E-9 CGDO=0.4E-9
.DC VIN -2.5 2.5 0.05
Figure 3. CMOS inverter transfer function and its various regions of operation

Figure 4. Cmos inverter complimentary currents
The operating point $V_{bias}$ is computed for the given example. The W/L ratio must use the $Leff = L - 2 * LD = 5.4u - 2*(0.5u) = 4.4u$, for both MN and MP transistors.

$$\beta_R = \beta_N / \beta_P = \frac{K_N(W / L)_N}{K_P(W / L)_P} = \frac{(40E - 6)(9.6u / 4.4u)}{(15E - 6)(25.8u / 4.4u)} = 1$$

$$V_{bias} = V_{SS} + (V_{DD} + V_{TP} + \sqrt{\beta_R V_{TN}}) / (1 + \sqrt{\beta_R}) = -2.5 + (2.5 - 1 + \sqrt{1}) / (1 + \sqrt{1}) = 0$$

The ac voltage gain can also be written as:

$$A_v = -[g_{mN} + g_{mP}][R_{ON} // R_{OP}]$$

where:

$$R_{ON} = 1 / (\beta_N I_{DSQ})$$

$$R_{OP} = 1 / (\beta_P I_{DSQ})$$

$$I_{DSQ} = I_N = I_P = (\beta_N / 2)(V_{bias} - V_{SS} - V_{TN})^2$$

$$g_{mN} = \sqrt{2\beta_N I_{DSQ}}$$

$$g_{mP} = \sqrt{2\beta_P I_{DSQ}}$$

For the given example:

$$I_{DSQ} = (\beta_N / 2)(V_{bias} - V_{SS} - V_{TN})^2 = (87.3E - 6 / 2)(0 - (-2.5) - 1)^2 = 98.3uA$$

$$R_{ON} = 1 / (\beta_N I_{DSQ}) = 1 / [(0.02)(98.2uA)] = .509M$$

$$R_{OP} = 1 / (\beta_P I_{DSQ}) = 1 / [(0.02)(98.2uA)] = .509M$$

$$\beta_N = K_N(W / L)_N = (40E - 6)(9.6u / 4.4u) = 87.3 \text{ uA} / \text{V}^2$$

$$\beta_P = K_P(W / L)_p = (15E - 6)(25.8u / 4.4u) = 87.95 \text{ uA} / \text{V}^2$$

$$g_{mN} = \sqrt{2\beta_N I_{DSQ}} = \sqrt{2(87.3E - 6)(98.2E - 6)} = 130.95 \text{ umho}$$

$$g_{mP} = \sqrt{2\beta_P I_{DSQ}} = \sqrt{2(87.95E - 6)(98.2E - 6)} = 131.43 \text{ umho}$$

$$A_v = -(g_{mN} + g_{mP})(R_{ON} // R_{OP}) = -(130.95 + 131.43)E - 6(.509M // .509M) = 66.77$$

The low frequency input resistance $R_{in} = \infty$, since the input is capacitive. The output resistance $R_{out} = (R_{ON} / R_{OP}) = .2545M$, see Figure 1(b). These calculations agree well with Pspice simulation results of:

**** SMALL-SIGNAL CHARACTERISTICS

$$V(2)/V_{IN} = -7.000E+01$$

INPUT RESISTANCE AT $V_{IN} = 1.000E+20$

OUTPUT RESISTANCE AT $V(2) = 2.536E+05$
3. High Frequency Small Signal Equivalent Circuit

Figure 5. CMOS inverter parasitic capacitances

Figure 5 shows all the parasitic capacitances in the common source amplifier. Figure 3 shows the high frequency small signal equivalent circuit of the common source amplifier circuit. Comparing Figure 3(b) and 3(c) one obtains:

\[ V_1 = V_s = V_i = V_{gs1} ; \quad V_2 = V_o \]

The current equation is:

\[ I_1 = s(C_{gs1} + C_{gs2})V_1 + s(C_{gd1} + C_{gd2})(V_1 - V_2) = s(C_{gs1} + C_{gs2} + C_{gd1} + C_{gd2})V_1 - s(C_{gd1} + C_{gd2})V_2 \]

\[ I_2 = (g_{m1} + g_{m2})V_1 + s(C_{gd1} + C_{gd2})(V_2 - V_1) + (g_{ds1} + g_{ds2} + sC_o)V_2 \]

\[ = [g_{m1} + g_{m2} - s(C_{gd1} + C_{gd2})]V_1 + [g_{ds1} + g_{ds2} + s(C_{gd1} + C_{gd2} + C_o)]V_2 \]
Figure 5. CMOS inverter high frequency equivalent circuit

The corresponding Y-parameter matrix is:

\[
Y = \begin{bmatrix}
  s(C_{gs1} + C_{gs2} + C_{gd1} + C_{gd2}) - s(C_{gd1} + C_{gd2}) \\
  g_{m1} + g_{m2} - s(C_{gd1} + C_{gd2}) & g_{ds1} + g_{ds2} + s(C_{gd1} + C_{gd2} + C_o)
\end{bmatrix}
\]
The overall voltage gain is:

\[
A_v = \frac{\frac{V_2}{V_1}}{y_{22} + Y_L} = \frac{g_{m1} + g_{m2} - s(C_{gd1} + C_{gd2})}{g_{ds1} + g_{ds2} + s(C_{gd1} + C_{gd2} + C_o)}
\]

\[
= \frac{g_{m1} + g_{m2}}{g_{ds1} + g_{ds2}} \left( \frac{1 - s(C_{gd1} + C_{gd2})}{g_{ds1} + g_{ds2} + s(C_{gd1} + C_{gd2} + C_o)} \right) = -A_v \left( \begin{array}{c} 1 - \frac{s}{z_1} \\ 1 - \frac{s}{p_1} \end{array} \right)
\]

where:

\[A_v = -\left( g_{m1} + g_{m2} \right) R_{out} \; ; \; R_{out} = \frac{1}{g_{ds1} + g_{ds2}} \]

\[z_1 = \frac{g_{m1} + g_{m2}}{C_{gd1} + C_{gd2}} \]

\[p_1 = \frac{1}{R_{out} C_{out}} \; ; \; C_{out} = C_{gd1} + C_{gd2} + C_o = C_{gd1} + C_{gd2} + C_{db1} + C_{db2} + C_L \]

\[w_{GBW} = A_v w_{BW} = \left( \left( g_{m1} + g_{m2} \right) R_{out} \right) \left( \frac{1}{R_{out} C_{out}} \right) = \frac{g_{m1} + g_{m2}}{C_{out}} \]

That is, the \(w_{GBW}\) is directly proportional to the transconductance of the driver transistor and inversely proportional to the total output capacitance. The Bode Plot is shown below:
The phase margin PM is the distance of the phase angle at the unity gain frequency with respect to –180 (in the non-inverting amplifier case) or with respect to 0 (in the inverting amplifier case). In our case this is with respect to 0. That is, the phase angle of the transfer function $A(s)$ at the unity gain frequency or the gain bandwidth frequency is also the phase margin, PM. This is obtained as follows:
\[ A(s) = \frac{A_0(1 - \frac{s}{z})}{(1 + \frac{s}{p_1})} \]

\[ A(jw_{\text{GBW}}) = \frac{A_0(1 - \frac{jw_{\text{GBW}}}{z})}{(1 + \frac{jw_{\text{GBW}}}{p_1})} \]

\[ \approx \frac{A_0(1 - \frac{jw_{\text{GBW}}}{z})}{p_1} \]

\[ \angle A(jw_{\text{GBW}}) = \angle A_0 + \angle(1 - \frac{jw_{\text{GBW}}}{z}) - \angle(\frac{jw_{\text{GBW}}}{p_1}) \]

\[ = 180 + \tan^{-1}\left(-\frac{w_{\text{GBW}}}{z}\right) - 90 = \text{PM} \]

\[ = 180 - \tan^{-1}\left(\frac{w_{\text{GBW}}}{z}\right) - 90 = \text{PM} \]

\[ \text{PM} = 90 - \tan^{-1}\left(\frac{w_{\text{GBW}}}{z}\right) \]

In the above analysis, the phase angle contribution of the zero, \( z \) is negative because it is a RHP zero. This is known as a non-minimum phase transfer function. This negative contribution causes the amplifier to be potentially unstable. The phase angle dynamic range of the amplifier with first order pole and a zero at the RHP is 180° rather than 0° if the zero is at LHP.

Without specifying the area and perimeter of the source and drain, only \( C_{gs} \) and \( C_{gd} \) are calculated by Pspice. From the common source experiment the parasitic capacitances had been determined. These are used to calculate the terminal capacitances for cmos inverter.
\[ C_O = C_{gd1} + C_{gd2} = 3.84 + 10.32 = 14.16 \text{fF} \]

Pspice extracted parameters:

\[ A_v = A_{v0} - 3 \quad f_{BW} = 44.212 \text{M} \]

\[ A_v = 0 \quad f_{GBW} = \infty = \text{graph asymptotic to 0db} \]

\[ \text{PM} = 0 \]

Comparing with theoretical calculation:

\[ w_{BW} = \frac{1}{R_0 C_O} = \frac{1}{(.2545E6)(14.16E -15)} = .2775E9 \]

\[ f_{BW} = \frac{w_{BW}}{2\pi} = \frac{.2775E9}{2\pi} = 44.186 \text{M} \]

\[ w_{GBW} = \frac{g_{m1} + g_{m2}}{C_O} = \frac{(130.95 + 131.43)E - 6}{14.16E - 15} = 18.53E9 = A_{v0} w_{BW} \]

\[ f_{GBW} = \frac{w_{GBW}}{2\pi} = \frac{18.53E9}{2\pi} = 2.95G \]

\[ z_1 = \frac{g_{m1} + g_{m2}}{C_{gd1} + C_{gd2}} = \frac{(130.95 + 131.43)E - 6}{C_O} = 18.53E9 = w_{GBW} \]

\[ f_{z_1} = \frac{z_1}{2\pi} = 2.95G = f_{GBW} \]

\[ \text{PM} = 90 - \tan^{-1}\left(\frac{w_{GBW}}{z}\right) = 90 - \tan^{-1}(1) = 45 \]

The discrepancy of the PM calculation is the result of zero occurring at \( w_{GBW} \). This causes the slope of bode plot to decrease to zero db/dec prior to intersecting the zero db line. As a result, the actual \( w_{GBW} \) occurs at \( \infty \) rather than at \( A_{v0} w_{BW} \) and PM=0.