Transmission Gate Characteristics

The transmission gate is on when en=5V and enb=0V, assuming the bulk of PMOS is connected to VDD(=5V) and the bulk of NMOS is connected to GND(=0V). In the on condition the output signal “out” will follows the input signal “in”. The operation of each transistor will first be analyzed. The NMOS switch will be analyzed by disconnecting the PMOS switch from the circuit. In Figure 1, the source is shown connected to the input “in”, due to symmetrical structure of MOS transistor the source and drain is not determined until the voltages are applied to the transistor. For NMOS the drain is connected to a higher potential than the source. In Figure 1 when the switch is on, the output V(out) follows the input V(in). That is, the V(out) is approximately equal but slightly less than V(in). Therefore, the source is connected to the “out” and V_{DS}=V(out)-V(in)≅0. With a small V_{DS}, the conducting NMOS transistor will be operating in the ohmic or non-saturated region. The NMOS will remain conducting as long as the gate to source voltage exceed the threshold voltage, V_{GS}\geq V_T. Since the bulk is not connected to the source, the bulk effect will increase the threshold voltage to about 1.5V. The calculation of the threshold voltage will be shown later. As the input voltage V(in) increases from 0 to 5V, the NMOS is on when V_{GS}= V(en)-V(out)\cong V(en)-V(in)=5-V(in)\cong 1.5 or V(in)\leq 3.5V. That is the NMOS switch will shut off when V(in)\geq 3.5V. This can be verified using Pspice simulation. In the Pspice coding, S and D is interchangeable. The code is given in listing 1(a). The 1G load resistance is required by Pspice to prevent a floating output node. Figure 2(a) shows the resistance value of the NMOS transistor as the input swing from 0 to 5V. The resistance becomes infinite at about 3.5V. The threshold voltage calculation will be illustrated. At V(in)=3.5V, the following voltages are obtained:

\begin{align*}
V_{DS}&=V(in)-V(out)\cong 0 = \geq V(in)\cong V(out)\cong V_S=3.5 \\
V_{GS}&=V_G-V_S=5-3.5=1.5 \\
V_{BS}&=V_B-V_S=0-3.5=-3.5
\end{align*}

The following parameters are obtained from scna2orbit level 2 spice parameter file:

V_{TON}=V_{TO}=0.8630
\[ \gamma = \text{GAMMA} = 0.4374 \]
\[ \phi = \text{PHI} = 0.6 \]

\[ V_{TN} = V_{TON} + \gamma(\sqrt{\phi - V_{BS}} - \sqrt{\phi}) = 0.8630 + 0.4374\left(\sqrt{0.6 - (3.5)} - \sqrt{0.6}\right) = 1.4098 \]

This voltage is very close to the assumed threshold voltage of 1.5V.

The PMOS switch can be analyzed in a similar manner. For PMOS the drain is connected to a lower voltage than the source. That is, in Figure 1, the drain of PMOS is actually connected to “out”. Again \( V_{DS} = V_{\text{out}} - V_{\text{in}} \geq 0 \). \(|V_{GS}| = |V_{\text{enb}} - V_{\text{in}}| = 0 - V_{\text{in}}| = V_{\text{in}} \geq |V_T| = |-1.5| = 1.5 \). That is, the PMOS switch is on as long as \( V_{\text{in}} \geq 1.5 \). It turns off when \( V_{\text{in}} \leq 1.5 \). This can be verified with Pspice simulation. Listing 1(b) shows the code. Figure 2(b) shows the on resistance of PMOS, which becomes infinite at about \( V_{\text{in}} = 1.5 \). The threshold voltage calculation will be illustrated. At \( V_{\text{in}} = 1.5 \), the following voltages are obtained:

\[ V_{DS} = V_{\text{out}} - V_{\text{in}} \geq 0 \Rightarrow V_{\text{out}} \geq V_{\text{in}} = V_S = 1.5 \]
\[ V_{GS} = V_G - V_S = 0 - 1.5 = -1.5 \]
\[ V_{BS} = V_B - V_S = 5 - 1.5 = 3.5 \]

The following parameters are obtained from scna2orbit level 2 spice parameter file:

\[ V_{TON} = V_{TO} = -0.9629 \]
\[ \gamma = \text{GAMMA} = 0.618 \]
\[ \phi = \text{PHI} = 0.6 \]

\[ V_{TP} = V_{TOP} - \gamma\left(\sqrt{\phi - V_{BS}} - \sqrt{\phi}\right) = -0.9629 - 0.618\left(\sqrt{0.6 + 3.5} - \sqrt{0.6}\right) = -1.7355 \]

This calculated agrees closely with the simulated result shown in Figure 2(b).

Figure 2(a) The On Resistance of the NMOS Transistor, Ronn.
Figure 2(b) The On Resistance of the PMOS Transistor, $R_{onp}$.

Figure 2(c) The Transmission Gate On Resistance $R_{on}$. $R_{on}(max) = 7.562k$. 
LISTING 1:
* tgate circuit
*Filename=tg_res.cir"

*Listing 1(a)
.LIB C:\e595\lib\myspice.lib
VDD vdd 0 DC 5
VSS vss 0 DC 0
VIN in 0 DC 0V
Ven en 0 DC 5V
*Venb enb 0 DC 0V

*MP1 out enb in vdd CMOSP W=6U L=2U
MN1 outn en in vss CMOSN W=6U L=2U

Rln outn 0 1G

.DC VIN 0 5V .01
.PROBE
.END

*Listing 1(b).
LIB C:\e595\lib\myspice.lib
VDD vdd 0 DC 5
VSS vss 0 DC 0
VIN in 0 DC 0V
*Ven en 0 DC 5V
Venb enb 0 DC 0V

MP1 outp enb in vdd CMOSP W=6U L=2U
*MN1 out en in vss CMOSN W=6U L=2U

RLp outp 0 1G

.DC VIN 0 5V .01
.PROBE
.END

*Listing 1(c)
.LIB C:\e595\lib\myspice.lib
VDD vdd 0 DC 5
VSS vss 0 DC 0
VIN in 0 DC 0V
Ven en 0 DC 5V
Venb enb 0 DC 0V

MP1 out enb in vdd CMOSP W=6U L=2U
The PMOS is cut off \((R_{onp} = \infty)\) for \(V_{in} \leq 1.5\) \(V\), and the NMOS is cutoff for \(V_{in} \geq 3.5\) \(V\). In the transmission gate configuration, the two transistors are connected in parallel. The combined parallel resistance is less than either the on resistance value. The combined resistance can be summarized as follows:

\[
\begin{align*}
0 \leq & V_{(in)} \leq 1.5 & R_{on} = R_{onn} & ;& \text{since } R_{onp} = \infty \\
1.5 < & V_{(in)} \leq 3.5 & R_{on} = R_{onn}/R_{onp} \\
V_{(in)} > & 3.5 & R_{on} = R_{onp} & ;& \text{since } R_{onn} = \infty
\end{align*}
\]

When the switch is on \(V_{(in)} = V_{(out)}\), hence \(V_{DS} = 0\). That is, the transistor is operating in the ohmic region. The drain current is given by:

\[
I_{DS} = K(W/L_{eff})(V_{GS} - V_T - V_{DS}/2)V_{DS} \approx K(W/L_{eff})(V_{GS} - V_T)V_{DS}
\]

\[
R_{DS} = \frac{V_{DS}}{I_{DS}} = \frac{1}{K(W/L_{eff})(V_{GS} - V_T)}
\]

To simplify the layout of transmission gate, the \((W/L)\) is usually chosen to be the same for both transistors. Since the transconductance \((K)\) of PMOS is less than for NMOS, the on resistance of PMOS is greater than that of the NMOS. That is, \(R_{onp} > R_{onn}\) for the same effective gate to source voltage.

For the given \(W/L\), the simulated combined parallel resistance of the transmission gate has a maximum value of 7.5622k. This maximum occurs when the NMOS transistor cutoff at \(V_{(in)} = 3.5\), since the combined resistance becomes \(R_{onp}\) which is decreasing in value thereafter. The theoretical value is calculated below:

At \(V_{(in)} = 3.5\)\(V\), the following voltages are obtained for the PMOS transistor:

\[
\begin{align*}
V_{DS} &= V_{(out)} - V_{(in)} \geq 0 = > V_{(out)} \geq V_{(in)} = V_s = 3.5 \\
V_{GS} &= V_G - V_s = 0 - 3.5 = -3.5 \\
V_{BS} &= V_B - V_s = 5 - 3.5 = 1.5
\end{align*}
\]

\[
V_{TP} = V_{TOP} - \gamma(V_{BS} - V_T) = -0.9629 - 0.618(\sqrt{0.6 + 1.5} - \sqrt{0.6}) = -1.37976
\]
The effective length of the transistor is given by:

$$L_{eff} = L - 2*LD = 2 - 2*(.309) = 1.382$$

where LD is obtained from scna20orbit level 2 spice parameter file

$$R_{DS} = \frac{V_{DS}}{I_{DS}} = \left| \frac{1}{K(W/L_{eff})(V_{GS} - V_T)} \right| = \frac{1}{(17.1E - 6)(6/1.382)(3.5 - (-1.37976))} = 6.35k$$

This calculated value is slightly lower than the simulated value of 7.5622k. The on resistance of the transmission gate can be reduced by increasing the (W/L) ratio. The on resistance is inversely proportional to the W/L ratio can be illustrated using Pspice simulation. The Pspice code is shown in LISTING 2. The simulation results are shown in Figure 3.

![Figure 3. Transmission gate characteristics.](image)

* tgate circuit
* Filename=tg_resm.cir"  

**LISTING 2:**

```plaintext
.Lib C:\e595\lib\mypspice.lib
VDD vdd 0 DC 5
VSS vss 0 DC 0
```
DIGITAL CIRCUITS IMPLEMENTATION WITH TRANSMISSION GATES

The digital gate implementation using transmission gates is based on shannon expansion theorem.

**Shannon expansion theorem:**

\[
F(x_1, x_2, ..., x_n) = x_1 F(1, x_2, x_3, ..., x_n) + x_1 F(0, x_2, x_3, ..., x_n) \\
F(x_1, x_2, ..., x_n) = x_1 x_2 F(1, 1, x_3, ..., x_n) + x_1 x_2 F(1, 0, x_3, ..., x_n) + x_1 x_2 F(0, 1, x_3, ..., x_n) + x_1 x_2 F(0, 0, x_3, ..., x_n)
\]

**Two-Input Universal Logic Module**

For function of two variables A, B

\[
F(A, B) = A F(1, B) + A F(0, B)
\]

<table>
<thead>
<tr>
<th>F(A,B)</th>
<th>NAME</th>
<th>F(0,B)</th>
<th>F(1,B)</th>
</tr>
</thead>
<tbody>
<tr>
<td>A B</td>
<td>AND</td>
<td>0</td>
<td>B</td>
</tr>
<tr>
<td>A + B</td>
<td>OR</td>
<td>B</td>
<td>1</td>
</tr>
<tr>
<td>A + B</td>
<td>NOR</td>
<td>B</td>
<td>0</td>
</tr>
<tr>
<td>A B</td>
<td>NAND</td>
<td>1</td>
<td>B</td>
</tr>
<tr>
<td>A B + A B</td>
<td>EXOR</td>
<td>B</td>
<td>B</td>
</tr>
<tr>
<td>A B + A B</td>
<td>NEXOR</td>
<td>B</td>
<td>B</td>
</tr>
</tbody>
</table>

**NOTE:** 0 = VSS, 1 = VDD
This shows that any two-input logic gate can be implemented using transmission gates and inverters only.

**Programmable Two-Input Universal Logic Module and MUX 4 to 1 or DEMUX 1 to 4**

\[ F(A,B) = \overline{\overline{A} B \overline{G_0}} + A \overline{B} G_1 \overline{\overline{G_1}} + A B G_2 + A B G_3 \]

<table>
<thead>
<tr>
<th>F(A,B)</th>
<th>NAME</th>
<th>G₀</th>
<th>G₁</th>
<th>G₂</th>
<th>G₃</th>
</tr>
</thead>
<tbody>
<tr>
<td>A B</td>
<td>AND</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>A + B</td>
<td>OR</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>A + B</td>
<td>NOR</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>A B</td>
<td>NAND</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>A B + A B</td>
<td>EXOR</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>A B + A B</td>
<td>NEXOR</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
</tbody>
</table>

The above universal logic module becomes a multiplexer 4-1 or demultiplexer 1-4, if we interpret the role of the input variables A, B as the two input select lines, with A the MSB and B the LSB. The \( G_0, G_1, G_2 \) and \( G_3 \) are the analog inputs. Since the transmission gate (TG) is symmetrical device we can interchange the role of input to output and vice versa.
Figure 1. Two-Input Universal Logic Module Using Transmission Gate.

\[ F(A,B) = A \cdot F(1,B) + \bar{A} \cdot F(0,B) \]
\[ F(A,B) = G_0(A \overline{B}) + G_1(\overline{A} B) + G_2(A \overline{B}) + G_3(A B) \]

Figure 2. Programmable Two-Input Universal Logic Module Using Transmission Gate.
Figure 3. The Basic Building Blocks (INV, and TG) used for Implementing NAND gate.
The functionality of the implemented NAND gate is verified with Pspice. The code is shown in LISTING 1, and simulated result is shown in Figure 4.

**LISTING 1:**
* 2 input nand circuit
* Filename=nand2_1.cir"

VDD vdd 0 DC 5V
VSS vss 0 DC 0

VIN1 in1 0 PWL(0,0V 2us,0V 2.01us,5V 12us,5V 12.01us,0V 1s,0V)
VIN2 in2 0 PWL(0,0V 1us,0V 1.01us,5V 8us,5V 8.01us,0V 1s,0V)

Xnand in1 in2 out vdd vss NAND

.SUBCKT NAND in1 in2 out vdd vss
Vhi hi 0 DC 5V
Xtg1 hi out in1b vdd vss TG
Xtg2 in2b out in1 vdd vss TG
Xinv1 in1 in1b vdd vss INVERTER
Xinv2 in2 in2b vdd vss INVERTER
. ENDS

.SUBCKT INVERTER in out vdd vss
MP1 out in vdd vdd CMOSP W=6U L=2U
bMN1 out in vss vss CMOSN W=6U L=2U
. ENDS INVERTER

.SUBCKT TG in out en vdd vss
MP1 out en_bar in vdd CMOSP W=6U L=2U
MN1 out en in vss CMOSN W=6U L=2U
Xinv en en_bar vdd vss INVERTER
. ENDS TG

*SCNA20 Orbit 2u technology Spice Parameters
.MODEL CMOSN NMOS LEVEL=2 PHI=0.600000 TOX=4.1000E-08 XJ=0.200000U
TPG=1
+ VTO=0.8630 DELTA=6.6420E+00 LD=2.4780E-07 KP=4.7401E-05
+ UO=562.8 UEXP=1.5270E-01 UCRIT=7.7040E+04 RSH=2.4000E+01
+ GAMMA=0.4374 NSUB=4.0880E+15 NFS=1.980E+11 NEFF=1.0000E+00
+ VMAX=5.8030E+04 LAMBDA=3.1840E-02 CGDO=3.1306E-10
+ CGSO=3.1306E-10 CGBO=4.3449E-10 CJ=9.5711E-05 MJ=0.7817
+ CJSW=5.0429E-10 MJSW=0.346510 PB=0.800000
* Weff = Wdrawn - Delta_W
*The suggested Delta_W is -5.4940E-07
.MODEL CMOSP PMOS LEVEL=2 PHI=0.600000 TOX=4.1000E-08 XJ=0.200000U
TPG=-1
+ VTO=-0.9629 DELTA=5.7540E+00 LD=3.0910E-07 KP=1.7106E-05
+ UO=203.1 UEXP=2.1320E-01 UCRIT=8.0280E+04 RSH=5.6770E+01
+ GAMMA=0.6180 NSUB=8.1610E+15 NFS=3.270E+11 NEFF=1.5000E+00
+ VMAX=9.9990E+05 LAMBDA=4.5120E-02 CGDO=3.9050E-10
+ CGSO=3.9050E-10 CGBO=4.1280E-10 CJ=3.2437E-04 MJSW=0.5637
+ CJSW=3.3912E-10 MJSW=0.275876 PB=0.800000
* Weff = Wdrawn - Delta_W
* The suggested Delta_W is -4.1580E-07

.TRAN 1ns 20us
.PROBE
.END

Figure 4. NAND gate Pspice simulation result.
Edge Triggered D Flip-Flop Implementation Using Transmission Gates

The operation of edge triggered DFF can be explained by tracing the D input signal as the clock signal goes from 0 to 1. The CLR input is assumed inactive (CLR=1). When CLK=0, transmission gates T1 and T4 are on, while T2 and T3 are off. In this state, D1=D, D2=D’, D3=Q’. G3 and G4 form a latch, latching the previous state Q(prev) of the DFF. When CLK=1, transmission gates T1 and T4 are off, while T2 and T3 are on. In this state, G1 and G2 form a latch latching the previous value of D, since D2=D’(prev), D1 =D(prev), the current input D is now disconnected from D1. D2=D1=D’(prev), and Q=D(prev). That is, the previous D input is latched on the rising edge of the CLK. Activating the CLR input (CLR=0), will force D2=1, Q’=1 regardless of the value of input D. The value of D2=1 is copied D3 and complemented to generate Q=0 in the next CLK rising edge. The operation of DFF with SET input is similar, except the activation of SET input (SET=0), will cause the DFF to set Q=1, and Q’=0.
Figure 5. Edge Triggered DFF with CLR/SET input Implementation Using TG
Figure 6. Edge Triggered DFF with CLR input Response.
Figure 7. Edge Triggered DFF with SET input Response.