Common Gate Amplifier

Figure 1(a) shows a common gate amplifier with ideal current source load. Figure 1(b) shows the ideal current source implemented by PMOS with constant gate to source voltage.

Figure 1. Common gate amplifier.
1. Low Frequency Small Signal Equivalent Circuit

Figure 2. Common gate amplifier low frequency small signal equivalent circuit.
Figure 2(a) and 2(b) show the low frequency small signal equivalent circuit. Figure 2(c) shows the two-port, its port variables assignment are as follows:

\[
Y_L = g_{ds2} \text{ (or } Z_L = r_{ds2}) ; \quad Y_S = \infty \text{ (or } Z_S = 0) \\
V_1 = V_i = -v_{gs1} , \quad V_2 = V_o
\]

From Figure 2(b), the current equations are derived to obtain the Y parameters:

\[
I_1 = g_{m1}V_i + g_{mb1}V_1 + g_{ds1}(V_i - V_2) = (g_{m1} + g_{mb1} + g_{ds1})V_i - g_{ds1}V_2 \\
I_2 = -(g_{m1} + g_{mb1})V_1 + g_{ds1}(V_2 - V_1) = -(g_{m1} + g_{mb1} + g_{ds1})V_1 + g_{ds1}V_2
\]

The corresponding Y-parameter matrix is,

\[
Y = \begin{bmatrix}
(g_{m1} + g_{mb1} + g_{ds1}) & -g_{ds1} \\
-(g_{m1} + g_{mb1} + g_{ds1}) & g_{ds1}
\end{bmatrix}
\]

\[
det Y = 0
\]

The input impedance of common gate amplifier is,

\[
Z_i = \frac{Y_{22} + Y_L}{det Y + y_{11}Y_L} = \frac{g_{ds1} + g_{ds2}}{0 + (g_{m1} + g_{mb1} + g_{ds1})g_{ds2}} \approx \frac{2g_{ds}}{g_m g_{ds}} = \frac{2}{g_m}
\]

This input impedance is low, since \(g_m\) is large. The output impedance of common gate amplifier is,

\[
Z_o = \frac{y_{11} + Y_S}{det Y + y_{22}Y_S} = \frac{1}{y_{22}} = \frac{1}{g_{ds1}}
\]

This output impedance is high, since \(g_{ds1}\) is very small. A common gate amplifier is primary used as impedance transformer from low to high impedance.

The voltage gain of common gate amplifier is,

\[
A_{v0} = \frac{-y_{21}}{y_{22} + Y_L} = \frac{g_{m1} + g_{mb1} + g_{ds1}}{g_{ds1} + g_{ds2}} = (g_{m1} + g_{mb1} + g_{ds1})R_{out} \approx g_{m1}R_{out}
\]

\[
\text{where: } R_{out} = \frac{Z_o}{Z_L} = \frac{1}{g_{ds1} + g_{ds2}}
\]

This voltage gain is practically the same as the common source amplifier, except for no signal inversion. The current gain of common gate amplifier is,

\[
A_i = \frac{-y_{21}Y_L}{det Y + y_{11}Y_L} = \frac{(g_{m1} + g_{mb1} + g_{ds1})g_{ds2}}{0 + (g_{m1} + g_{mb1} + g_{ds1})g_{ds2}} = 1
\]
2. High Frequency Small Signal Equivalent Circuit

![Common gate amplifier](image)

Figure 3. Common gate amplifier parasitic capacitances.

Figure 3 shows all the parasitic capacitances needed for high frequency model.

Figure 4(a) shows the high frequency small signal equivalent circuit of common gate amplifier. The two-port assignment is shown in Figure 4(b).

The network current equation is:

\[
\begin{align*}
I_1 &= (g_{m1} + g_{mb1})V_1 + sC_i V_1 + g_{ds1}(V_1 - V_2) = (g_{m1} + g_{mb1} + g_{ds1} + sC_i)V_1 - g_{ds1}V_2 \\
I_2 &= -(g_{m1} + g_{mb1})V_1 + g_{ds1}(V_2 - V_1) + sC_o V_2 = -(g_{m1} + g_{mb1} + g_{ds1})V_1 + (g_{ds1} + sC_o)V
\end{align*}
\]

The corresponding Y-parameter matrix is:

\[
Y = \begin{bmatrix}
g_{m1} + g_{mb1} + g_{ds1} + sC_i & -g_{ds1} \\
-(g_{m1} + g_{mb1} + g_{ds1}) & g_{ds1} + sC_o
\end{bmatrix}
\]

\[
\text{det}Y = (g_{m1} + g_{mb1} + g_{ds1} + sC_i)(g_{ds1} + sC_o) - g_{ds1}(g_{m1} + g_{mb1} + g_{ds1})
\]

\[
= s[g_{ds1}C_i + (g_{m1} + g_{mb1} + g_{ds1})C_o] + s^2 C_o C_i
\]
The output impedance is given by:

$$Z_o = \frac{\sigma_{22} + Y_L}{\text{det}Y + \sigma_{11} Y_L} = \frac{(g_{ds1} + sC_o) + g_{ds2}}{s[g_{ds1}C_i + (g_{m1} + g_{mb1} + g_{ds1})C_o] + s^2C_o C_i + (g_{m1} + g_{mb1} + g_{ds1} + sC_i)g_{ds2}}$$

$$= \frac{(g_{m1} + g_{mb1} + g_{ds1})g_{ds2} + s[(g_{ds1} + g_{ds2})C_i + (g_{m1} + g_{mb1} + g_{ds1})C_o] + s^2C_o C_i}{(g_{m1} + g_{mb1} + g_{ds1})g_{ds2}}$$

The output impedance is given by:
\[ Z_o = \frac{y_{11} + Y_s}{\det Y + y_{22} Y_s} = \frac{1}{\frac{1}{y_{22}} + \frac{1}{g_{ds1} + sC_o}} \]

The voltage gain is given by:

\[ A_v = \frac{V_2}{V_1} = \frac{-y_{21}}{y_{22} + Y_L} = \frac{g_{m1} + g_{mb1} + g_{ds1}}{(g_{ds1} + sC_o) + g_{ds2}} = \frac{g_{m1} + g_{mb1} + g_{ds1}}{(g_{ds1} + g_{ds2} + sC_o)} \]

\[ = \frac{(g_{m1} + g_{mb1} + g_{ds1})R_{out}}{1 + sC_o R_{out}} = \frac{A_{V0}}{1 + \frac{s}{p_1}} \]

The bandwidth is defined by the dominant pole \( p_1 \). That is,

\[ w_{BW} = p_1 = \frac{1}{R_{out} C_o} \]

\[ f_{BW} = f_{-3db} = f_{p1} = \frac{w_{BW}}{2\pi} \]

The gain bandwidth is given by:

\[ w_{GBW} = A_{V0} w_{BW} = (g_{m1} + g_{mb1} + g_{ds1})R_{out} \frac{1}{R_{out} C_o} = \frac{(g_{m1} + g_{mb1} + g_{ds1})}{C_o} \]

\[ f_{GBW} = \frac{w_{GBW}}{2\pi} \]

The phase margin PM for the non-inverting amplifier, which the case here, is the distance of the phase angle at the unity gain (or 0db) frequency (\( f_{GBW} \)) to \(-180\). That is,
\[ \angle A(jw_{GBW}) = -180 + PM \]
\[ A(s) = \frac{A_v_0}{1 + \frac{s}{p_1}} \]
\[ \angle A(s) = \angle A_v_0 - \angle \left(1 + \frac{jw_{GBW}}{p_1}\right) = -180 + PM \]
\[ = 0 - \tan^{-1}\left(\frac{w_{GBW}}{p_1}\right) = -180 + PM = 180 - \tan^{-1}(A_v_0) \]
\[ PM = 180 - \tan^{-1}\left(\frac{w_{GBW}}{p_1}\right) = 180 - \tan^{-1}\left(\frac{w_{GBW}}{w_{BW}}\right) = 180 - \tan^{-1}(A_v_0) \]

The transfer signal is a single pole with no zero. The PM is always greater 90°. Hence it is stable.

**Common Gate Amplifier Experiments**

3. **Common Gate Amplifier Biasing and Low Frequency Small Signal Parameters Determination.**

The DC or large signal transfer characteristic is difficult to obtain analytically. The reasons are the gate to source voltage and the threshold voltage changes with the input voltage. From Figure 1, these voltages are given by:

\[ V_{GS1} = V_{GI} - V_i \]
\[ V_{BS} = V_{SS} - V_i \]

Instead of obtaining the complete DC transfer characteristic, only the bias point or operating point is of interest. The operating point should lie in the region when both transistors are in saturation. The goal is to obtain the upper and lower bound of the saturation region.

M2, the PMOS transistor in Figure 1 is in saturation when the condition is satisfied.

\[ |V_{GSP}| - |V_{TP}| < |V_{DSP}| \]
\[ |V_{G2} - V_{DD}| - |V_{TP}| < |V_{O} - V_{DD}| \]
\[ |0 - V_{DD}| - 1 < |V_{O} - V_{DD}| \]
\[ V_{DD} - 1 < V_{DD} - V_{O} \]
\[ V_{O} < 1 \]

M1, the NMOS transistor in Figure 1 is in saturation when:
\[ V_{GSN} - V_{TN} = V_{DSN} \]
\[ V_{G1} - V_i - V_{TN} < V_O - V_i \]
\[ V_{G1} + V_{TN} = 1 + 1 = 2 \]
\[ V_{GSN} - V_{TN} > 0.3 \]
\[ V_{G1} - V_i - V_{TN} > 0.3 \]
\[ V_{G1} > 0.3 + V_i + V_{TN} = 0.3 + 0 + 1 = 1.3 \text{ ; at bias point } V_i = 0 \]

That is,
\[ 1.3 < V_{G1} < 2 \]

This defines the range of \( V_{G1} \) when \( V_{G2} = 0 \) to guarantee that both transistors are in saturation, select say \( V_{G1} = 1.5 \). With this value selected, PSpice simulation is conducted to determine the actual operating point, the bias voltage of the input signal. Initially, the PSpice file simply enters a guess value of the bias voltage. This bias will affect the AC response but not the DC response. The bias voltage is obtained by selecting a point at the middle of the steepest slope. The simulation shows that this bias voltage is \(-1.4903\). This information is entered in the PSpice file and re-run to obtain the proper AC response. The operating point and small signal parameters are determined as follows:

The threshold voltage is computed at the operating point as follows:

\[ V_{BS} = V_B - V_S = V_{SS} - V_i = -2.5 - (-1.4903) = -1.0097 \]
\[ V_{TN} = V_{TO} + \gamma(\sqrt{\phi - V_{BS}} - \sqrt{\phi}) = 1 + 1(\sqrt{0.6 - (-1.0097)} - \sqrt{0.6}) = 1.4909 \]

The operating point current is

\[ \beta_N = K_N \left( \frac{W}{L} \right)_N = 40E - 6 \left( \frac{9.6E - 6}{(5.4 - 1)E - 6} \right) = 87.27E - 6 \]
\[ I_{DSQ} = I_N = I_1 = I_2 = I_p \]
\[ = \left( \frac{\beta_N}{2} \right)(V_{GSN} - V_{TN})^2 = \left( \frac{\beta_N}{2} \right)(V_{G1} - V_i - V_{TN})^2 \]
\[ = \left( \frac{87.27E - 6}{2} \right)(1.5 - (-1.4903) - 1.4909)^2 = 98.21 \mu A \]

The transconductances and resistances are computed:
\[ g_{m1} = g_{mN} = \sqrt{2/\beta_N I_{DSQ}} = \sqrt{2(87.27E-6)(98.2E-6)} = 130.95E-6 = 130.95 \text{umho} \]

\[ g_{mb1} = \frac{\gamma}{2/\phi - V_{BS}} g_{m1} = \frac{1}{2 \sqrt{0.6 - (-1.0097)}} (130.95E-6) = 51.7625E-6 = 51.7625 \text{umhoA} \]

\[ r_{ds1} = R_{ON} = \frac{1}{\lambda_N I_{DSQ}} = \frac{1}{(0.02)(98.21E-6)} = 0.509E6 = 0.509 \text{M} \]

\[ g_{ds1} = \frac{1}{r_{ds1}} = 1.9642E-6 \]

\[ r_{ds2} = R_{OP} = \frac{1}{\lambda_P I_{DSQ}} = \frac{1}{(0.02)(98.21E-6)} = 0.509E6 = 0.509 \text{M} \]

\[ g_{ds2} = \frac{1}{r_{ds2}} = 1.9642E-6 \]

\[ R_{out} = (R_{ON}/R_{OP}) = 0.2545E6 = 0.2545 \text{M} \]

\[ Z_i = \frac{g_{ds1} + g_{ds2}}{(g_{m1} + g_{mb1} + g_{ds1})g_{ds2}} = \frac{(1.9642 + 1.9642)E-6}{(130.95 + 51.7625 + 1.9642)E-6(1.9642E-6)} = 1.08E4 \]

\[ A_V = (g_{m1} + g_{mb1} + g_{ds1})R_{out} = (130.95 + 51.7625 + 1.9642)E-6(0.2545E6) = 47 \]

\[ A_{Vdb} = 20 \log_{10}(A_V) = 20 \log_{10}(47) = 33.44 \text{ db} \]

The PSpice simulation shows that

\[ Z_i = 1.032 \times 10^4 \]

\[ Z_o = 2.543 \times 10^5 \]

\[ A_V = 33.756 \text{db} \]

*PSpice file for NMOS Common Gate Amplifier with PMOS Current Load
*Filename="Lab3.cir"
VIN 1 0 DC -1.4903VOLT AC 1V
VDD 3 0 DC 2.5VOLT
VSS 4 0 DC -2.5VOLT
VG1 5 0 DC 1.5VOLT
VG2 6 0 DC 0VOLT
M1 2 5 1 4 MN W=9.6U L=5.4U
M2 2 6 3 3 MP W=25.8U L=5.4U

.MODEL MN NMOS VTO=1 KP=40U
+ GAMMA=1.0 LAMBDA=0.02 PHI=0.6
+ TOX=0.05U LD=0.5U CJ=5E-4 CJSW=10E-10
+ U0=550 MJ=0.5 MJSW=0.5 CGSO=0.4E-9 CGDO=0.4E-9

.MODEL MP PMOS VTO=-1 KP=15U
+ GAMMA=0.6 LAMBDA=0.02 PHI=0.6
+ TOX=0.05U LD=0.5U CJ=5E-4 CJSW=10E-10
+ U0=200 MJ=0.5 MJSW=0.5 CGSO=0.4E-9 CGDO=0.4E-9
V(2)/VIN = 4.894E+01

INPUT RESISTANCE AT VIN = 1.032E+04

OUTPUT RESISTANCE AT V(2) = 2.543E+05
4. Common Gate Amplifier High Frequency Model Experiments

The parasitic capacitances will be determined to check the theory against Pspice simulation results. The capacitances are determined at the operating point. The reverse bias are first calculated. For PMOS,

\[ V_{BD} = V_B - V_D = V_{DD} - V_O = 2.5 - 0.56 = 1.94 \] (entered as negative PMOS polarity are reversed)

\[ V_{BS} = 0 \]

For NMOS

\[ V_{BD} = V_B - V_D = V_{SS} - V_O = 2.5 - 0.56 = -3.06 \]

\[ V_{BS} = V_B - V_{SS} = V_I - 2.5 = -1.4903 = -1.0097 \]

* VO=0.56 is the output voltage at operating point.
The MATLAB program is invoked to obtain the parasitic capacitances.

For NMOS,

\[ [CGS, CGD, CBD, CBS] = \text{cap}(9.6, 5.4, -3.06, -1.0097) \]

\[ CGS = 23.2704 \text{fF} \quad CGD = 3.84 \text{fF} \quad CBD = 19.3375 \text{fF} \quad CBS = 43.2441 \text{fF} \]

For PMOS,

\[ [CGS, CGD, CBD, CBS] = \text{cap}(25.8, 5.4, -1.94, 0) \]

\[ CGS = 62.5392 \text{fF} \quad CGD = 10.32 \text{fF} \quad CBD = 55.4944 \text{fF} \quad CBS = 152.02 \text{fF} \]

In the first Pspice simulation, only the Cgs and Cgd are included. That is, the output capacitance is calculated as follow:

\[ C_o = C_{gd1} + C_{gd2} = 3.84 \text{fF} + 10.32 \text{fF} = 14.16 \text{fF} \]
The theoretical bandwidth is calculated as follows:

\[ w_{BW} = \frac{1}{\frac{1}{R_{out} C_O} = \frac{1}{(.2545E6)(14.16E -15)} = 277.49E6} \]

\[ f_{BW} = \frac{w_{BW}}{2\pi} = \frac{277.49E6}{2\pi} = 44E9 = 44M \]

\[ w_{GBW} = \frac{(g_{m1} + g_{mb1} + g_{ds1})}{C_O} = \frac{(130.95 + 51.7625 + 1.9642)E - 6}{14.16E -15} = 13.042E9 \]

\[ f_{GBW} = \frac{w_{GBW}}{2\pi} = \frac{13.04E9}{2\pi} = 2.077E9 = 2.077G \]

\[ PM = 180 - \tan^{-1}\left(\frac{W_{GBW}}{W_{BW}}\right) = 180 - \tan^{-1}\left(\frac{13.042E9}{277.49E6}\right) = 91.22 \]

The Pspice simulation results are:

\[ f_{BW} = f_{\lambda db} = 44.452M \]

\[ f_{GBW} = 2.1779G \]

\[ PM = 91.163 \]

To include the effect of all the parasitic capacitances, the area and perimeter of the source and drain of each transistor are included in the PSpice netlist. The output capacitance is re-calculated to include all the parasitic capacitances.

\[ C_O = C_{gd1} + C_{db1} + C_{gd2} + C_{db2} + C_L \]
\[ = (3.84 + 19.3375 + 10.32 + 55.4944)F = 88.9919fF \]

\[ w_{BW} = \frac{1}{\frac{1}{R_{out} C_O} = \frac{1}{(.2545E6)(88.9919E -15)} = 44E6} \]

\[ f_{BW} = \frac{w_{BW}}{2\pi} = \frac{44E6}{2\pi} = 7E9 = 7M \]

\[ w_{GBW} = \frac{(g_{m1} + g_{mb1} + g_{ds1})}{C_O} = \frac{(130.95 + 51.7625 + 1.9642)E - 6}{88.9919E -15} = 2.075E9 \]

\[ f_{GBW} = \frac{w_{GBW}}{2\pi} = \frac{2.075E9}{2\pi} = 0.3305E9 = 330.5M \]

\[ PM = 180 - \tan^{-1}\left(\frac{W_{GBW}}{W_{BW}}\right) = 180 - \tan^{-1}\left(\frac{2.075E9}{44E9}\right) = 91.215 \]

The Pspice simulation results are:
$f_{BW} = 6.6343 \text{M}$

$g_{GBW} = 305.995 \text{M}$

$PM = 91.169$

*PSpice file for NMOS Common Gate Amplifier with
*PMOS Current Load
*Filename="Lab31.cir"
VIN 1 0 DC -1.4903VOLT AC 1V
VDD 3 0 DC 2.5VOLT
VSS 4 0 DC -2.5VOLT
VG1 5 0 DC 1.5VOLT
VG2 6 0 DC 0VOLT
M1 2 5 1 4 MN W=9.6U L=5.4U AD=40.32P AS=40.32P PD=27.6U PS=27.6U
M2 2 6 3 3 MP W=25.8U L=5.4U AD=108.36P AS=108.36P PD=60U PS=60U

.model MN NMOS VTO=1 KP=40U
+ GAMMA=1.0 LAMBDA=0.02 PHI=0.6
+ TOX=0.05U LD=0.5U CJ=5E-4 CJSW=10E-10
+ U0=550 MJ=0.5 MJSW=0.5 CGSO=0.4E-9 CGDO=0.4E-9
.model MP PMOS VTO=-1 KP=15U
+ GAMMA=0.6 LAMBDA=0.02 PHI=0.6
+ TOX=0.05U LD=0.5U CJ=5E-4 CJSW=10E-10
+ U0=200 MJ=0.5 MJSW=0.5 CGSO=0.4E-9 CGDO=0.4E-9
*Analysis
.dc VIN -2.5 2.5 0.05
.tf V(2) VIN
.ac dec 100 1HZ 10GHZ
.probe
.end