

ECE 7530
ADVANCED DIGITAL DESIGN USING VHDL
Winter' 11

This is a 4-credit hour graduate course in an integrated lecture and laboratory format. The course is design to teach digital design using VHDL language. The emphasis is on writing codes that can be synthesized. To learn how to create packages and libraries of re-useable models that has been tested and successfully synthesized to create more complex circuits. To use iterative regular structures suitable for VLSI circuits. The students will learn how to decompose a complicated system like CISC/RISC computer architectures to a manageable interconnected components using structural modeling. CADENCE CAD tools are used to show the steps of creating a VLSI circuits using VHDL language.

Course Objectives: To learn digital VLSI circuit design using VHDL.

Textbook :

“Digital Systems Design Using VHDL” by Charles H. Roth Jr.

Handouts will be given with emphasis on synthesis using Cadence Cad Tools

Instructor: Dr. Pepe Siy
Rm 3125 Engineering
Phone: (313)577-3841
E-mail: psiy@ece.eng.wayne.edu

TA: Gurwinder Bawa
Rm 3355 Engineering
Phone: (313)577-5796
E-mail: du6668@wayne.edu

Lecture:	Wednesday 1165 Main	10:40-12:30 AM
Lab:	2360 Engineering (UNIX LAB)	
	Monday	10:40-12:30 AM
	Others	By appointment only

Materials to be covered

1. Introduction to VHDL
2. VHDL Data Types
3. Packages and Libraries
4. Structural Modeling
5. VHDL Opertators
6. Model Structure
7. Sequential Machine VHDL Implementation
8. Resolving Multi-Signal Drivers
9. Data Objects
10. Looping Constructs
11. Chip Level Modelling
12. Digital Design

13. CISC Computer Design

Grading Policy

Individual Lab-10%

Project-20%

Mid-term –30%

Final – 40%

Grades:

A	A-	B+	B	B-	C+	C	F
≥ 90	≥ 80	≥ 70	≥ 60	≥ 50	≥ 40	≥ 30	< 30

Schedule:

Mid-Term : 3/2/11 (Wednesday), 10:40-12:30 AM

Final: 4/27/11 (Wednesday), 10:40-12:30 AM