I. (A)

<table>
<thead>
<tr>
<th>Time (t(ns))</th>
<th>Current Value</th>
<th>Queued Values</th>
</tr>
</thead>
<tbody>
<tr>
<td>t(ns)</td>
<td>x(t)</td>
<td>y(t)</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>∆</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>10</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>20</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>20+∆</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>30</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>40</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

II.

ENTITY circuit IS
  PORT(X, CLK: IN STD_LOGIC; Z: OUT STD_LOGIC);
END circuit;
ARCHITECTURE dflow OF circuit IS
  SIGNAL d1, d2, clkb, q1, q1b, q2, q2b: STD_LOGIC;
BEGIN
  D1<=q1b OR q2;
  D2<=X AND q2b;
  Z<=q1 OR q2b;
  Clkb <= NOT CLK;
END PROCESS (clk)
BEGIN
IF (clk'EVENT AND clk='1') THEN
  q1<=d1;
END IF;
END PROCESS;
q1b<=NOT q1;
PROCESS (clkb)
BEGIN
  IF (clkb'EVENT AND clkb='1') THEN
    q2b<=d2;
  END IF;
END PROCESS;
q2b<=NOT q2;
END dflow;

III.

LIBRARY IEEE, VHDL;
USE IEEE.STD_LOGIC_1164.ALL;
USE VHDL.DIGITAL.ALL;
ENTITY circuit IS
  PORT(X, CLK: IN STD_LOGIC; Z: OUT STD_LOGIC);
END circuit;
ARCHITECTURE struct OF circuit IS
  *Component Declaration Section
  COMPONENT and2c
    PORT(x,y:IN STD_LOGIC;z:OUT STD_LOGIC);
  END COMPONENT and2c;
  COMPONENT or2c
    PORT(x,y:IN STD_LOGIC;z:OUT STD_LOGIC);
  END COMPONENT or2c;
  COMPONENT invc
    PORT(x:IN STD_LOGIC;y:OUT STD_LOGIC);
  END COMPONENT invc;
  COMPONENT dffc
    PORT(d,clk:IN STD_LOGIC;q, qb:OUT STD_LOGIC);
  END COMPONENT dffc;
  *Component Specification Section
  FOR U1,U2:  or2c USE ENTITY VHDL.or2(or2_arch);
  FOR U3: and2c USE ENTITY VHDL.and2(and2_arch);
  FOR U4: invc USE ENTITY VHDL.inv(inv_arch);
  FOR DFF1,DFF2: dffc USE ENTITY VHDL.dff(dff_arch);
  *Internal Signal Declaration Section
  SIGNAL d1, d2, clkb, q1, q1b, q2, q2b: STD_LOGIC;
BEGIN
*Component Instantiation Section
DFF1: dffc PORT MAP(d1,CLK,q1,q1b);
DFF2: dffc PORT MAP(d2, clkb, q2,q2b);
U1: or2c PORT MAP(q1b, q2b, d1);
U2: or2c PORT MAP(q1, q2b, Z);
U3 and2c PORT MAP(X, q2b, d2);
U4 invc PORT MAP(CLK, clkb);
END struct;

IV.
LIBRARY IEEE
USE IEEE.STD_LOGIC_1164.ALL;
ENTITY signal_generator IS
  PORT (reset, ph1, ph2:OUT STD_LOGIC);
END signal_generator;

ARCHITECTURE beh OF signal_generator IS
BEGIN
  reset<=’1’, ‘0’ AFTER 10 ns;
  PROCESS
  BEGIN
    ph1<=’1’, ‘0’ AFTER 10 ns;
    ph2<=’0’, ‘1’ AFTER 12 ns, ‘0’ AFTER 18 ns;
    WAIT FOR 20 ns;
  END PROCESS;
END beh;