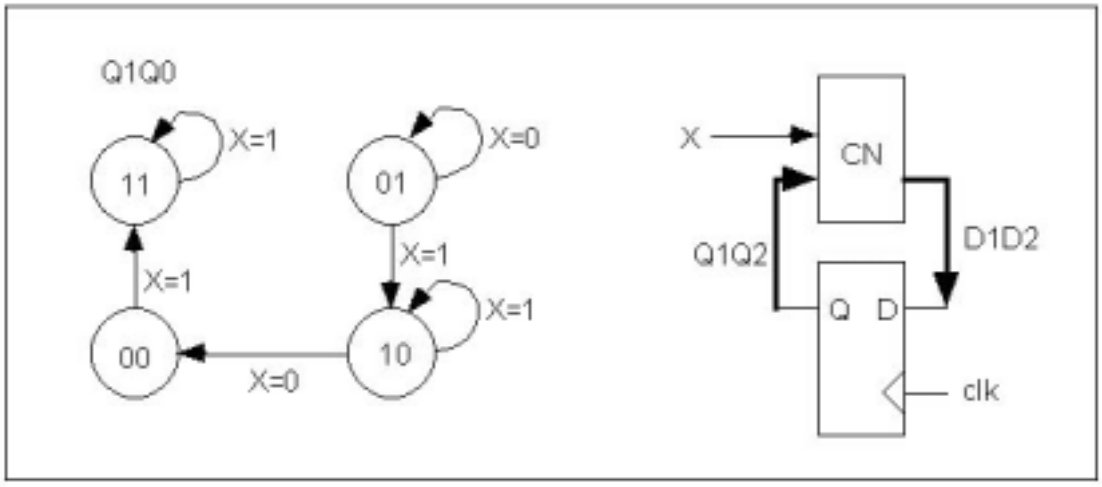
12.0 Digital Design

Problem with Unsynchronized Inputs

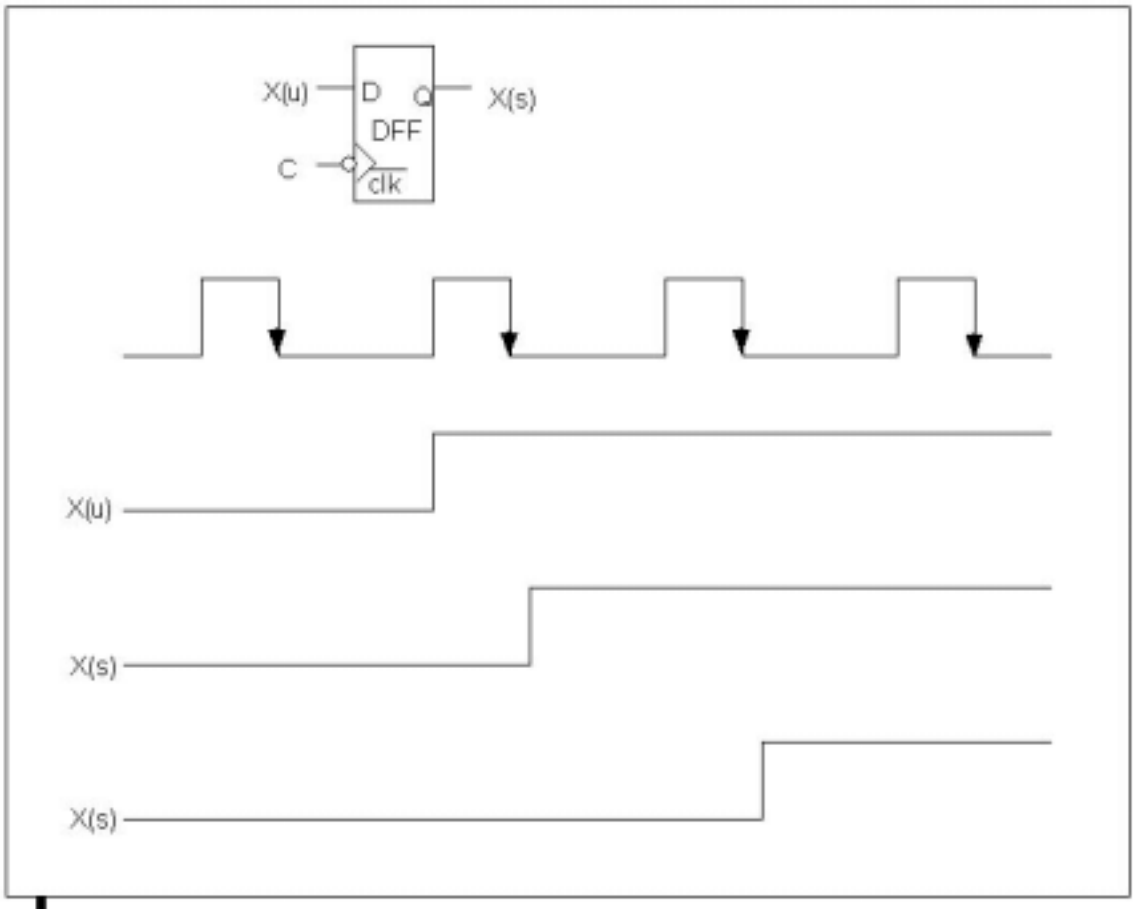
If the finite state machine (FSM) input X is not synchronized with the FSM clock clk, then X may change at any time during the clock period. If this is the case then it is not possible to guarantee satisfaction of the setup and hold requirements of the state register and the output, regarless of how large the clock period (T), or how much delay is inserted in the signal paths. If the input X to a DFF changes during the required setup and hold interval. Three things may happen:

1. The DFF may remain in the same state S0.
2. The DFF may change to next state S1.
3. The DFF may enter a prolong period of transition, where it oscillates between the 0 and 1 regions, before resolving to 0 or 1.



If the input X changes at a time that causes D=f(X,Q) to change during the required setup and hold interval, then some bits of Q may respond to old value of X and some to the new value. For the given FSM at state Q=Q1Q2=01, if X changes from 0 to 1 but the change occurs at such a time the first bit , Q1, of the state register responds to the old value of X, while the second bit, Q2, responds to the new value. The FSM would then make a transition to state 00. Then the FSM goes to state 11 in the next clock period. But it should have gone to, and stayed in state 10.

Input Synchronizer using DFF



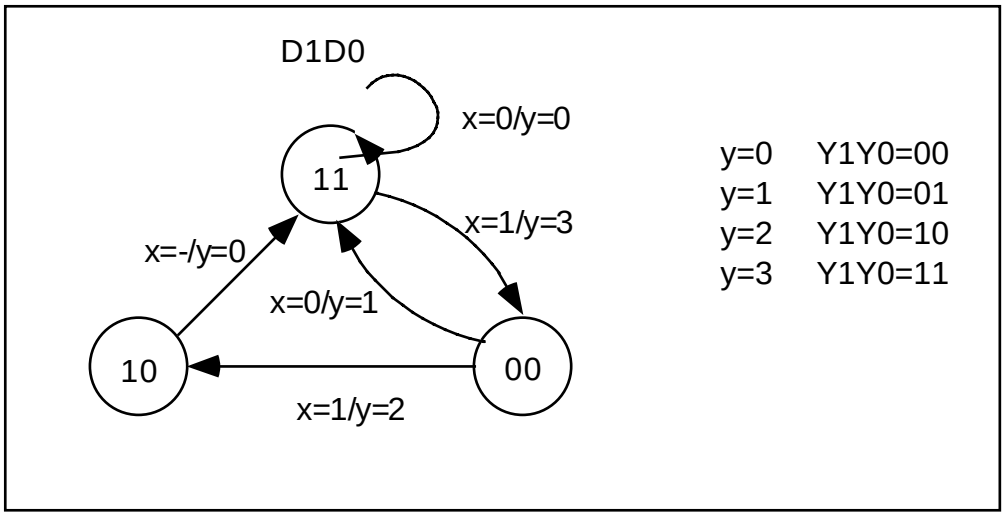
There are two possible response due to X(u) 0 to 1 transition:

X(s) => 1 immediately
X(s) => 1 delayed by one clock period.

Design Example

The process of designing a FSM may be decomposed into four steps:

1. Construct a sequential machine that exhibits the desired sequential behavior.
2. Code the sequential machine.
3. Design a combinational network to implement the next state and output functions.
4. Establish timing.



X is assumed synchronized to the clock.

Q1Q0

X	**00**	**01**	**11**	**10**
0	1	X	1	1
1	1	X	0	1

D1=(X and Q0)'

Q1Q0

X	**00**	**01**	**11**	**10**
0	1	X	1	1
1	0	X	0	1

D0=X' + Q1 and Q0'

Q1Q0

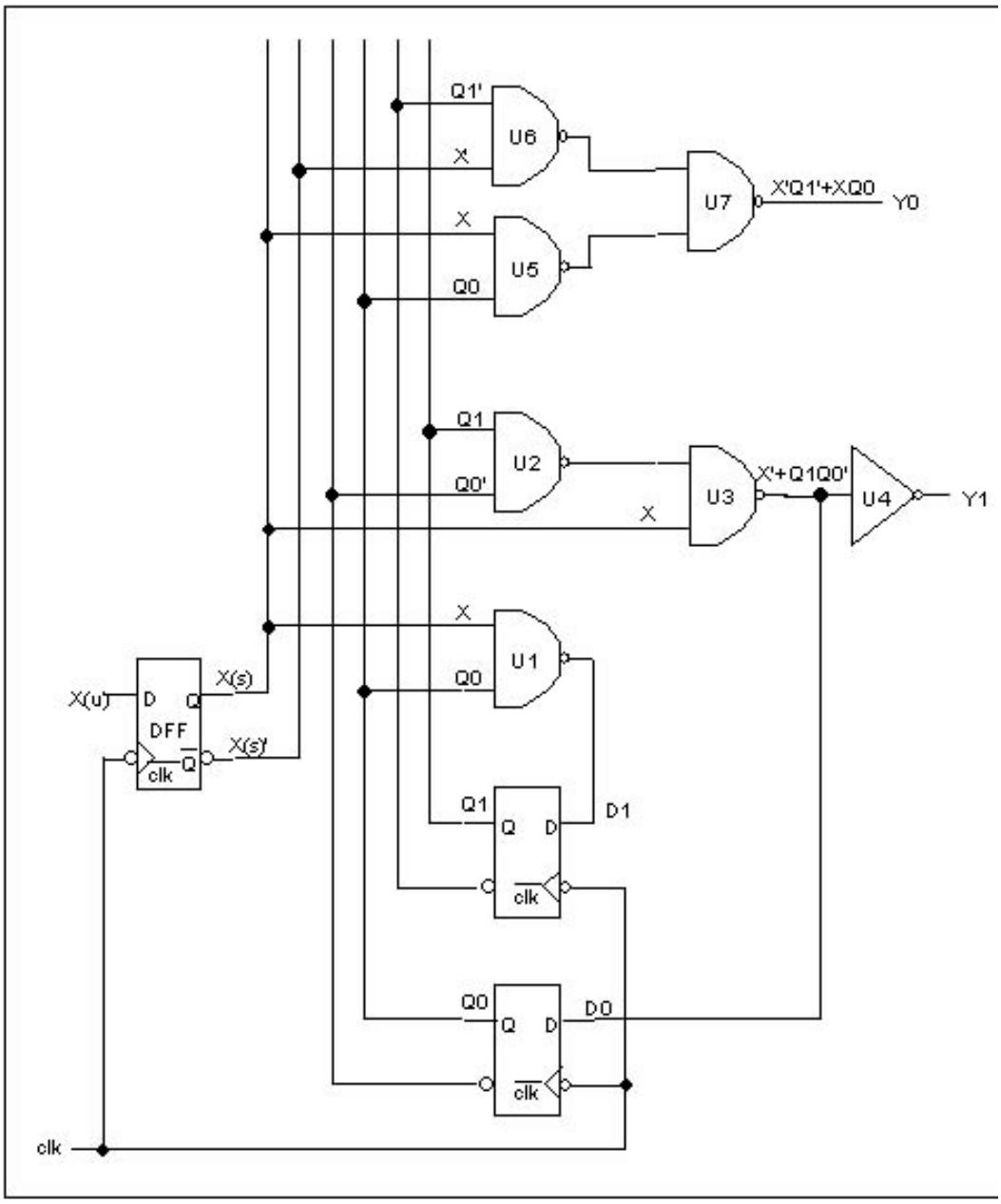
X	**00**	**01**	**11**	**10**
0	0	X	0	0
1	1	X	1	0

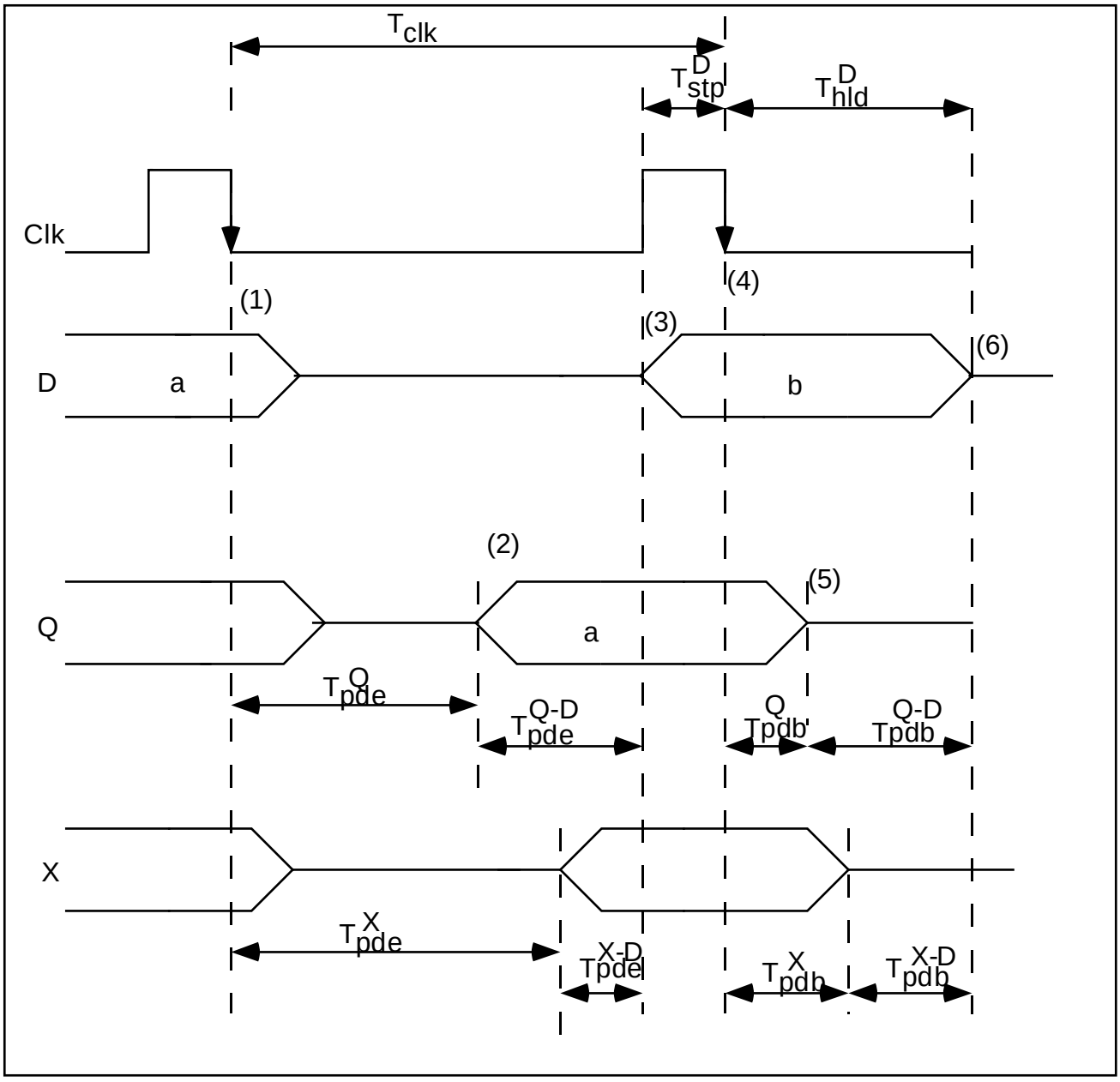
Y1=D0'

Q1Q0

X	**00**	**01**	**11**	**10**
0	1	X	0	0
1	0	X	1	0

Y0=X' and Q0' + X and Q0


Q1'
U6
X
X'Q1'+XQ0
U7
Y0
X
U5
Q0
Q1
U2
Q0'
X'+Q1Q0'
U3
U4
Y1
X
X
U1
Q0
X(u)
D
Q
X(s)
DFF
clk
Q
X(s)'
Q1
Q
D
D1
clk
Q0
Q
D
D0
clk
clk



Sequence of Events

D=f(X,Q)

In (1) Clk↓ latch the value of D=a (the next state), which causes a change in Q after T_{pde}^{Q} later at (2), the change in Q subsequently change D=b (the subsequent state) after $T_{pde}^{Q\text{-}D}$ later at (3), D=b is then latch T_{stp}^{D} later at (4). That is

$$T_{clk} \geq \left(T_{pde}^{Q}\right)_{max} + \left(T_{pde}^{Q\text{-}D}\right)_{max} + \left(T_{stp}^{D}\right)_{min}$$

At (4) D=b is latch, Q start to change T_{pdb}^{Q} later at (5). When Q change it also cause D start to change

T_{pdb}^{Q-D} later at (6), which is the end of hold time of D=b.

Setup Time Constraint

$$Q => D: \; T_{clk} \geq \left(T_{pde}^{Q}\right)_{max} + \left(T_{pde}^{Q-D}\right)_{max} + \left(T_{stp}^{D}\right)_{min}$$
$$X => D: \; T_{clk} \geq \left(T_{pde}^{X}\right)_{max} + \left(T_{pde}^{X-D}\right)_{max} + \left(T_{stp}^{D}\right)_{min}$$

Hold Time Constraint

Must ensure that the changes at Q and X that occur at the beginning of each clock period do not propagate to D too quickly.

$$Q => D: \left(T_{pdb}^{Q}\right)_{min} + \left(T_{pdb}^{Q-D}\right)_{min} \geq \left(T_{hld}^{D}\right)_{min}$$
$$X => D: \left(T_{pdb}^{X}\right)_{min} + \left(T_{pdb}^{X-D}\right)_{min} \geq \left(T_{hld}^{D}\right)_{min}$$

Consider Constraint on output Y=f(X,Q)

$$Q => Y: \; T_{clk} \geq \left(T_{pde}^{Q}\right)_{max} + \left(T_{pde}^{Q-Y}\right)_{max} + \left(T_{stp}^{Y}\right)_{min}$$
$$X => Y: \; T_{clk} \geq \left(T_{pde}^{X}\right)_{max} + \left(T_{pde}^{X-Y}\right)_{max} + \left(T_{stp}^{Y}\right)_{min}$$
$$Q => Y: \left(T_{pdb}^{Q}\right)_{min} + \left(T_{pdb}^{Q-D}\right)_{min} \geq \left(T_{hld}^{D}\right)_{min}$$
$$X => Y: \left(T_{pdb}^{X}\right)_{max} + \left(T_{pdb}^{X-Y}\right)_{max} \geq \left(T_{hld}^{Y}\right)_{min}$$

Device and Signal Specifications:

$$\text{Requirements}: T_{stp}^{D} \geq 3\text{ns} \quad T_{hld}^{D} \geq 0\text{ ns (Next state Data duration)}$$
$$\text{Requirements}: T_{h}^{clk} \geq 6\text{ ns} \quad T_{l}^{clk} \geq 7\text{ ns (Clock duration)}$$
$$\text{Guarantees}: 3\text{ ns} \leq T_{pd}^{Q} \leq 10\text{ ns (DFF delay)}$$
$$\text{Guarantees}: 2\text{ ns} \leq T_{pd}^{gate} \leq 6\text{ ns (Gate delay)}$$
$$\text{Guarantees}: T_{pdb}^{X} \geq 4\text{ ns} \quad T_{pde}^{X} \leq 20\text{ ns (Input delay)}$$
$$\text{Requirements}: T_{stp}^{Y} \geq 10\text{ ns} \quad T_{hld}^{Y} \geq 5\text{ ns (Output duration)}$$

Setup Constraint Determine Tclk

This determine the operating speed of your design. It involves finding the longest propagation delay path.

Q=>D:

Q1 => U2 => U3 => D0
Q0 => U1 => D1

Q0’ => U2 => U3 => D0

X =>D:

X => U1 => D1

X => U3 =D0

Q => Y:

Q0’ => U2 =>U3 => U4 => Y1 *

Q0 => U5 => U7 => Y0

Q1’ => U6 => U7 => Y0

Q1 => U2 => U3 => U4 => Y1 *

X => Y:

X => U8 => U6 => U7 => Y0 *

X =>U5 => U7 => Y0

X => U3 => U4 => Y1

* The worst case has three gate propagation delay

X=> Y0 (worst case)

$$T_{clk} \geq \left(T_{pde}^{X}\right)_{max} + \left(T_{pde}^{X-Y}\right)_{max} + \left(T_{stp}^{Y}\right)_{min} = 20 + (6+6+6) + 10 = 48ns$$

Hold Inequalitites

To Satisfy the Hold Inequalitiesinvolve searching for the shortest signal path.

Candidate shortest path are:

Q0 => U1 => D1	$3+2 > 0 = (T_{hld}^{D})_{min}$
X => U1 => D1	$4+2 > 0 = (T_{hld}^{D})_{min}$
Q1 => U6 => U7 => Y0	$3 + 2 + 2 > 5 = (T_{hld}^{Y})_{min}$
X => U5 => U7 => Y0	$4 + 2 + 2 > 5 = (T_{hld}^{Y})_{min}$

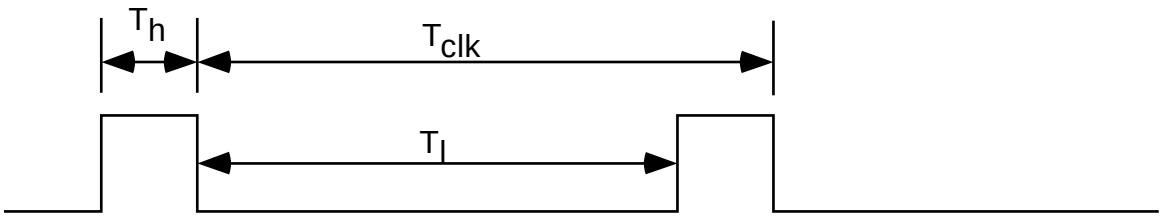
All hold inequalities are satisfied. If any of the hold inequalities had not been satisfied, it would have been necessary to insert delay in the offending path using 2 inverters in series.

In conclusion the FSM will operate properly if

$T_{clk} \geq 48$ ns

$6ns \leq T_h^{clk} \leq 41$ ns

$7ns \leq T_i^{clk}$


T_h
T_{clk}
T_l