Lab 9: VHDL Datapath Design

The datapath is a major part of CPU. It includes a Register File and a Function Unit. The function unit consists of an ALU and a Shifter Register.

Based on the 16x16 Register file, you have to make some modifications. Figure. 1 is the modified register file.

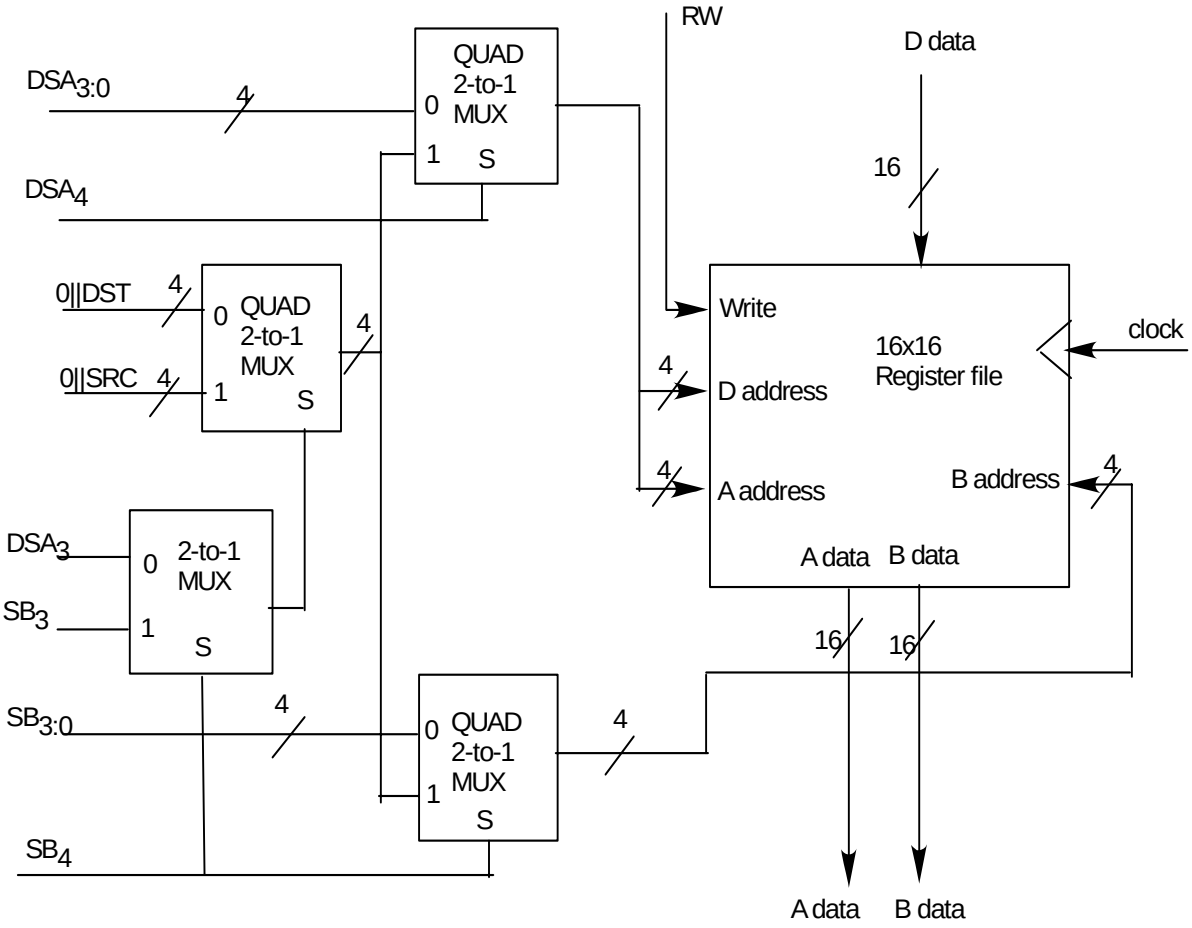

Figure1. Block diagram of the modified diagram.

A quad 2-to-1 multiplexer is attached to each of the two address inputs to the register file, to select between an address from the microcontroller and an address from the instruction. There is a 5-bit signal in the microcontroller for the combined destination and source address DSA, in addition another 5-bit signal for the B address SB. The first bit of each of these fields selects the register file address source. If the first bit is 0 it selects the microcontroller(MC), else it selects the instruction(IR). If an instruction is selected, whether it is DST or SRC is determined by an additional quad 2-to-1 multiplexer. This

multiplexer is controlled by the second bit of the DSA or SB field, depending on which of them has 1 as the first bit. **Only one of the signals DSA and SB is allowed to have a 1 in the first bit**, thereby ensuring that the proper second bit is used to determine the register address. A 0 is appended to the left of the 3-bit fields DST and SRC to cause them to address R0 through R7. In addition to the first bit, which selects the address source, the addresses from the microcontroller contain four bits so that all 16 registers can be reached. The final change to the register is to replace the storage elements for R0 in the file with open circuits on the lines that were their inputs and with constant zero values on the lines that were their outputs.

DSA[4:3]	**SB[4:3]**	**DSA source**	**SB source**
10	0X	0//DST	SB[3:0]
11	0X	0//SRC	SB[3:0]
0X	10	DSA[3:0]	0//DST
0X	11	DSA[3:0]	0//SRC
0X	0X	DSA[3:0]	SB[3:0]

The block diagram and symbol for a 16x16 Register file is showing in figure 2.

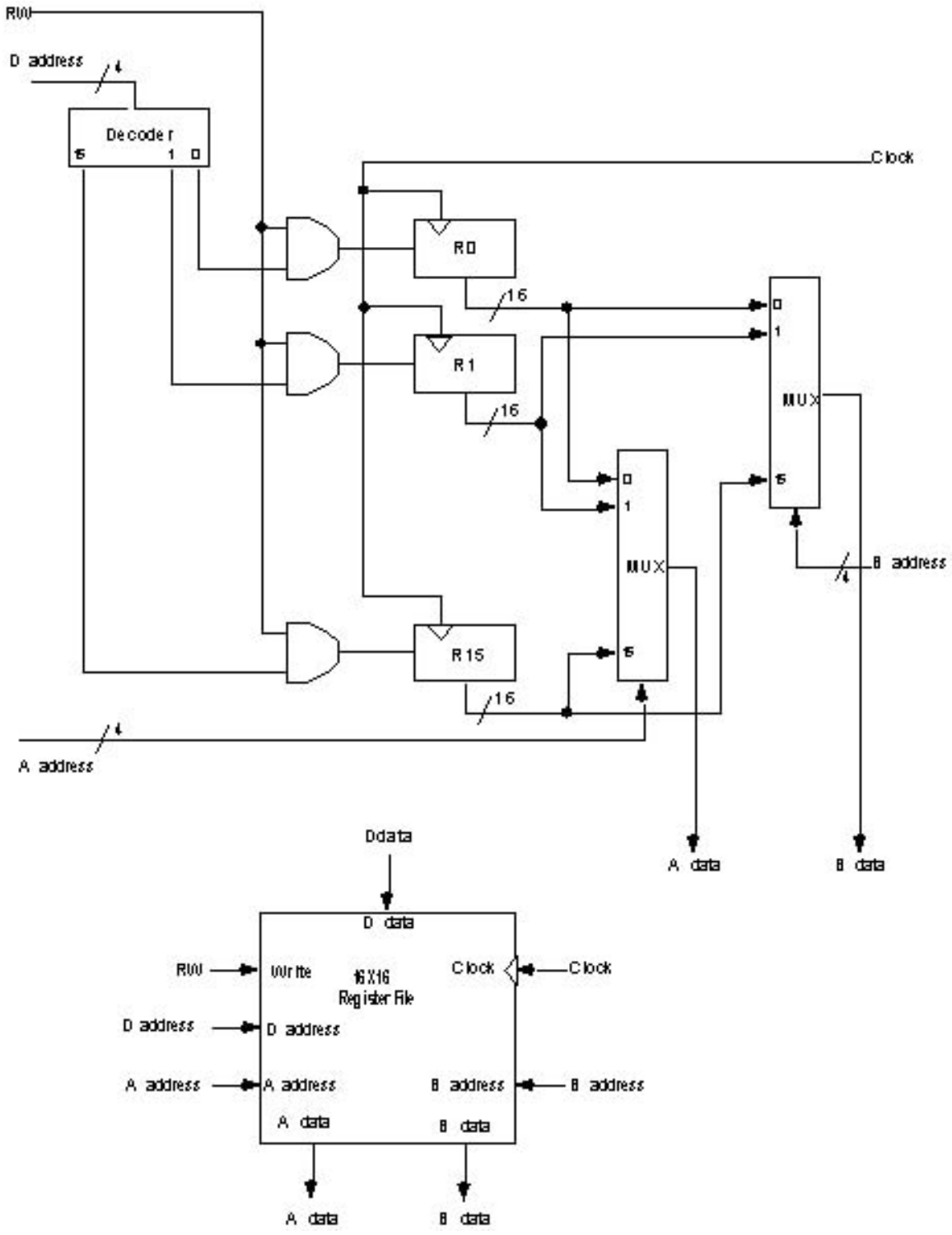

Figure2. Block diagram and symbol for a 16x16 register file

For the function unit, you may use the ALU and shift register designs you created before. The block diagram of a function unit is showing below.

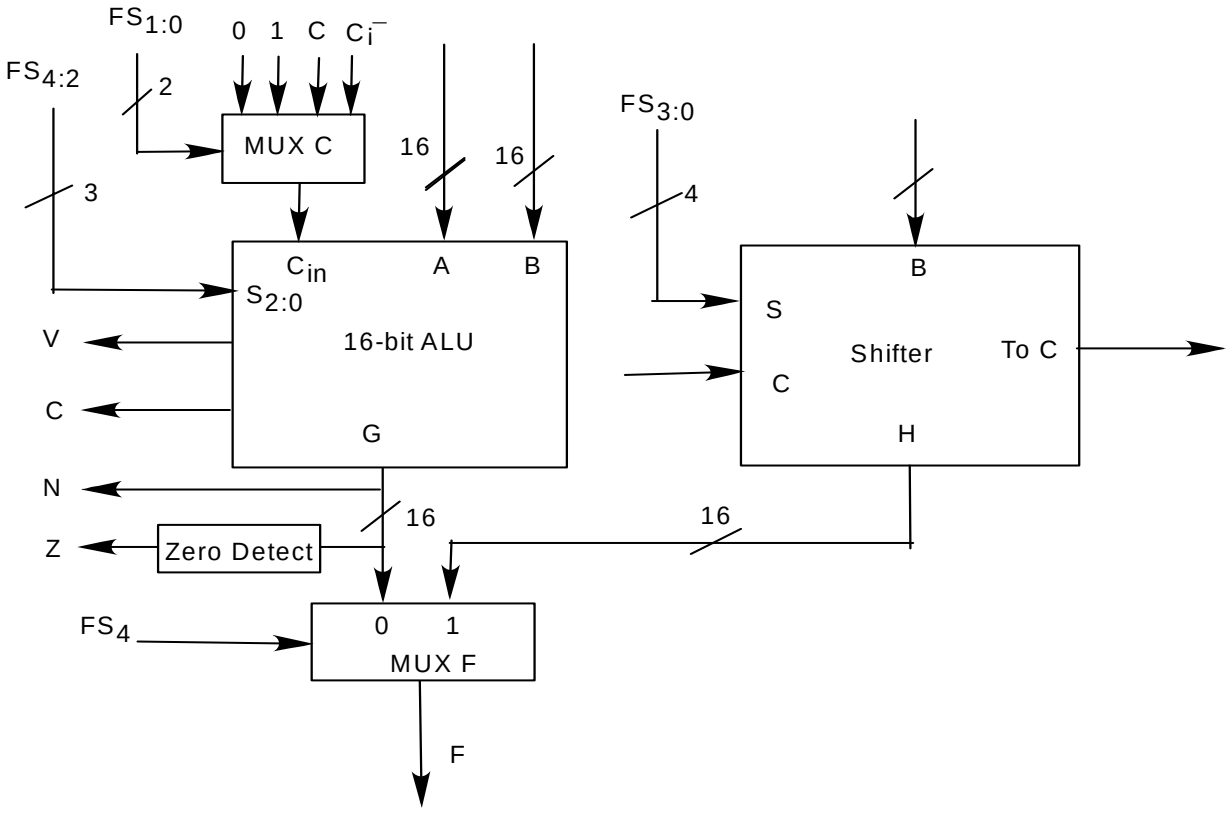

Figure 3. Block diagram of the function unit

Function Table for the function unit

FS	**Operation**	**FS**	**Operation**
000000	A	100000	B
000001	A+1	101000	lsl B
000100	A+B(ADD)	100100	lsr B
000101	A+B+1	101001	asl B
000110	A+B+C(ADDC)	100101	asr B
001000	A+B’	101010	rol B
001001	A+B’+1(SUB))	100110	ror B
001011	(A+B’+1+C’)(SUBB)	101011	rolc B
001100	A-1	100111	rorc B
010000	A∧B		
010101	A∨B		
011000	A⊕B		
011101	A’		

FS[5] =Func/Shift & Rotate Select
0: Func
1: Shift & Rotate
FS[4:2] = S[2:0] Func select in Lab8
FS[1;0] = Carry select
00:0
01:1
10:C
11:C’

16-bit Data Path block diagram:

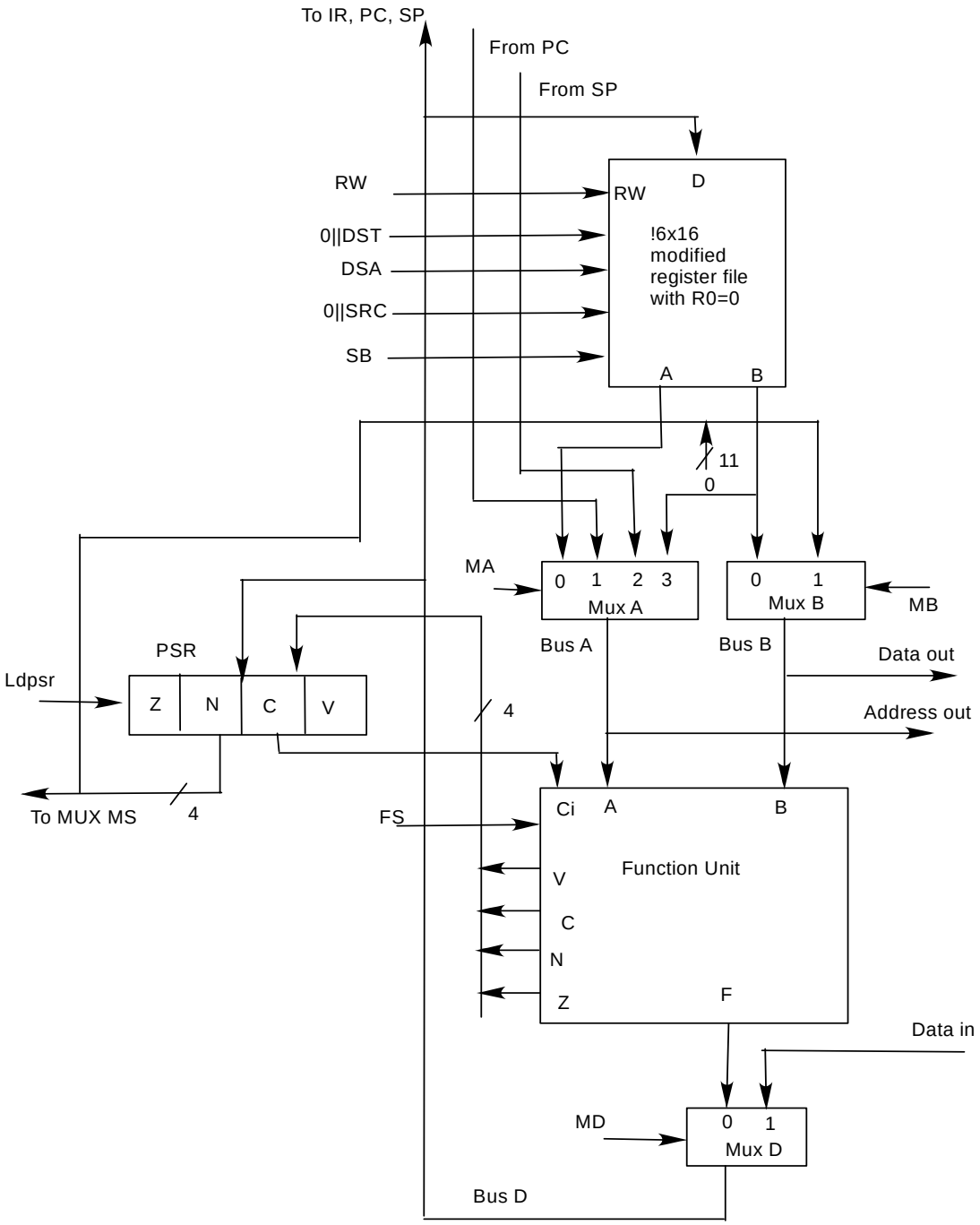

Figure 4. Block diagram for the datapath.

TASKS:

(a) Write the vhdl code to model the above datapth
(b) Write the testbench to simulate your vhdl model
(c) Synthesize your vhdl model, i.e. generate schematic