Lab 6: VHDL Up/Down Counter Design

Objective: Design, synthesize, and simulate a counter with up down selection mode.

Note: While using "buildgates" to synthesize the code. Please change the second console command

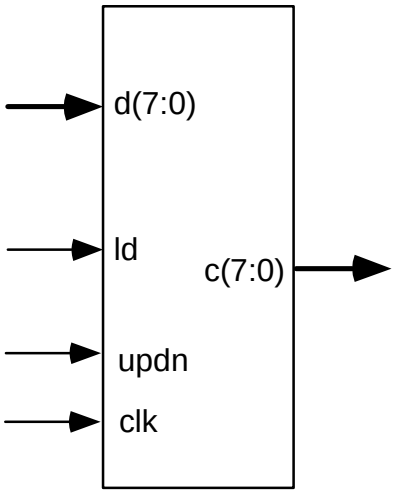
"set_global hdl_vhdl_environment synopsys"

To

"set_global hdl_vhdl_environment common".

8-bit Counter Specification:

This counter is loaded with an initial count value and count down by one until zero.



Condition	Operation	Comment
ld =’1’	c <=d	load
clk ↑ & updn= ’1’	c <= c + 1	increment counter
clk ↑ & updn= ’0’	c <= c - 1	Decrement counter

TASKS:

(a) Write the vhdl entity “count” and architecture that model the above 8-bit counter
(b) Write the testbench “count_test”. Simulate your vhdl model
(c) Synthesize your vhdl model, i.e. generate schematic.