Lab 6: VHDL Up/Down Counter Design

**Objective:** Design, synthesize, and simulate a counter with up down selection mode.

**Note:** While using "buildgates" to synthesize the code. Please change the second console command

"set_global hdl_vhdl_environment synopsys"

To

"set_global hdl_vhdl_environment common".

**8-bit Counter Specification:**
This counter is loaded with an initial count value and count down by one until zero.

<table>
<thead>
<tr>
<th>Condition</th>
<th>Operation</th>
<th>Comment</th>
</tr>
</thead>
<tbody>
<tr>
<td>ld = '1'</td>
<td>c &lt;= d</td>
<td>load</td>
</tr>
<tr>
<td>clk &amp; updn = '1'</td>
<td>c &lt;= c + 1</td>
<td>increment counter</td>
</tr>
<tr>
<td>clk &amp; updn = '0'</td>
<td>c &lt;= c - 1</td>
<td>Decrement counter</td>
</tr>
</tbody>
</table>

**TASKS:**
(a) Write the vhdl entity “count” and architecture that model the above 8-bit counter
(b) Write the testbench “count_test”. Simulate your vhdl model
(c) Synthesize your vhdl model, i.e. generate schematic.