Lab 2: VHDL Code Synthesis Using Ambit BuildGates

Invoke Ambit BuildGates and start the synthesizing process. 

Note: You need to be at the ~/cadence/vhdl directory.

emitsun1% cd 
cadence/vhdl 
emitsun1% bga Shell -gui

A graphical user interface will open up like the one shown below

Enter the following set of commands to get your netlist. You have to read in your VHDL from bottom to top so that all modules are defined before they are used.

ac_shell[1]>read_tlf ami06.tlf
ac_shell[2]>set_global hdl_vhdl_environment synopsys (this controls which ieee.std libraries are
included)
ac_shell[3]>read vhdl xorgate/src/xor.vhd

ac_shell[4]>do_build_generic  (this will do the synthesis)
ac_shell[5]>do_optimize   (this will map the synthesized logic to ami06 std cells)
ac_shell[6]>write_verilog xorgate/src/xor.v

Now you can view the schematic of your design by Double click the module “xorgate[xorgate](m)” in the right window.