Lab1: VHDL Design Coding, Compilation, and Simulation

Logging in Instructions

Cadence tools can be accessed from Engg 2360

A. Setting up the environment

1. open .cshrc file

Doubleclick on the " ab1234's Home" folder on your desktop (" ab1234" should be your AccessID), Click " View" and check " Show Hidden Files". Scroll down to find the .cshrc file. The file is currently ReadOnly. Rightclick on the file and choose " Properties". Go to the " Permissions" tag and check " Owner >Write" .Click " Close". Now again right click on the file but choose " Open with Text Editor". This will open the .cshrc file in text editor.

```
I. Find the following line:
    source /usr/local/etc/ALLSET
II. comment out that line, i.e. put # sign in front, like this:
     #source /usr/local/etc/ALLSET
III. add these two lines:
     source /opt/cds/class/cds_setup

     source /opt/cds/class/setup_files/vhdl/.vhdl_setup
```

Finally, source the ***.cshrc*** file(type "source .cshrc") or open a new terminal.

2. Now start a terminal window by right click on the desktop and choose " Open Terminal" and you should be able to create the *cadence* directory under you home directory.

gfxlab11% **cd $HOME**

gfxlab11% **mkdir cadence**

3. Create *vhdl* directory under *cadence* directory.

gfxlab11% **cd $HOME/cadence**

gfxlab11% **mkdir vhdl**

gfxlab11% **cd vhdl**

4. Copy some option files

gfxlab11% cp $NCVHDL/cds.lib $CDSVHDL

gfxlab11% cp $NCVHDL/hdl.var $CDSVHDL

B. Writing VHDL code

1.setup directory for the design **xorgate**

```
gfxlab11% cd $CDSVHDL
gfxlab11%  mkdir xorgate
gfxlab11%  cd xorgate
gfxlab11% mkdir src
```

2. Using a text editor, type your VHDL code. Here is a VHDL code for *xorgate* that you can use. This code is saved as *xor.vhd* under *src* directory.

```
----- Start of VHDL code -----
LIBRARY ieee;
use ieee.std_logic_1164.all;
ENTITY xorgate IS
  port (A:          IN    std_logic;
        B:          IN    std_logic;
        F:          OUT   std_logic);
END xorgate;
ARCHITECTURE syn OF xorgate IS
BEGIN
p1 : PROCESS (A, B)
  BEGIN  --  PROCESS p1
    F <= A XOR B;
  END PROCESS p1;
END syn;
----- End of VHDL code -----
```

C. Compiling the VHDL code

1. Before compiling your VHDL code, make sure you are at the ***$HOME/cadence/vhdl*** directory.

```
gfxlab11%  cd  $HOME/cadence/vhdl
gfxlab11% nclaunch &
```

The NCLaunch command opens up the NCLaunch graphical user interface (GUI) main window. The main window(NCL window) is composed of a menu bar, toolbar icon strip, file browser, design area and console window as shown in the figure below.

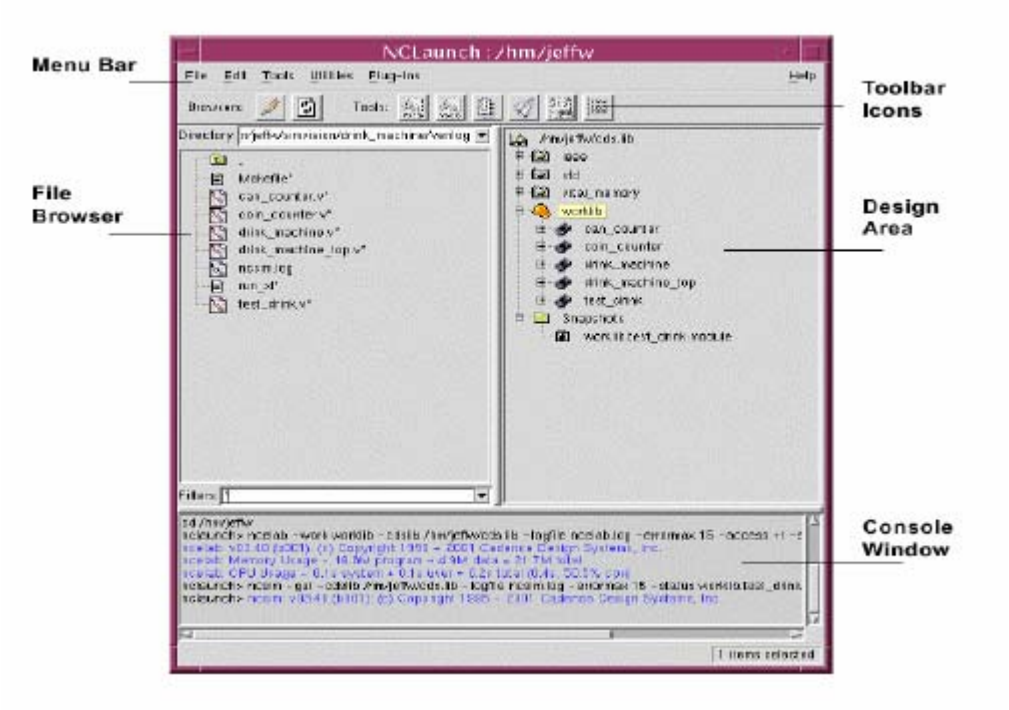


Figure 1. NCL Window

The main NCLaunch window is divided into the following components:

- Menu Bar and Tool Bar--Provide the commands and fast action buttons that let you manipulate design elements and start the various tools.
- File Browser--The pane on the left side of the window displays the files in the file system.
- Design Area--The pane on the right side of the window displays objects in the libraries.
- Console Window--Displays output from tools, and allows you to input commands.

2. Compile the VHDL code.

Select your VHDL source file *xor.vhd* from File Browser area. (expand xorgate folder then expand src)

To invoke VHDL compiler

- (NCL)Tools > VHDL Compiler.

The Compile VHDL form appears.

♦ Click the *OK* button.

The results of the compilation appear in the Console Window of the NCLaunch window. After the source files have been compiled, you can click the plus sign (+) to the left of *worklib* in the Design Area. This expands the *worklib* library and lists the VHDL design units that you have compiled. NOTE: by default *worklib* is the same as current directory which is $HOME/cadence/vhdl

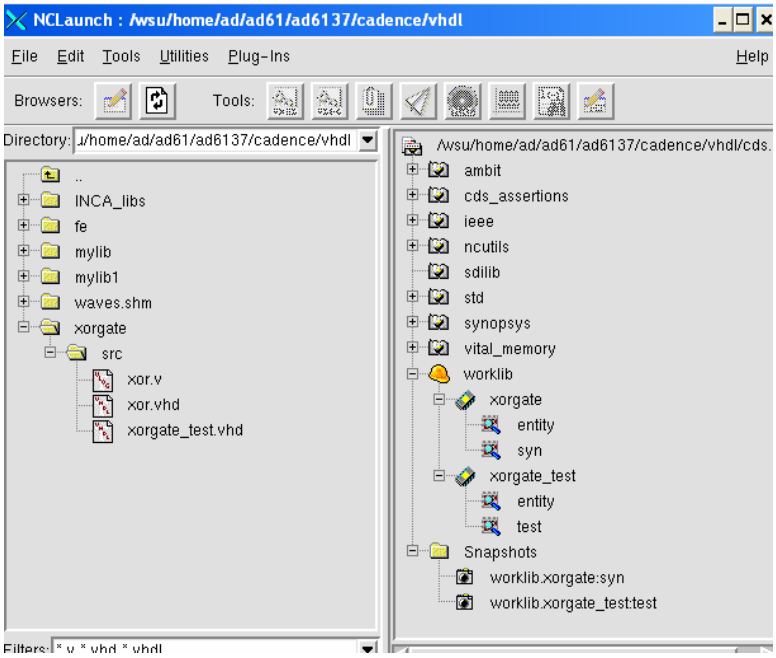


Figure 2. NCL Window showing file structure

3. If there is no error reported, go to the next step; otherwise, read the error messages and fix your VHDL codes accordingly. Then, recompile the code again until there is no error.

D. Elaborating the Design

After compiling the VHDL source code, you must elaborate the design using a program called *NCELAB*. The elaboration process constructs a design hierarchy based on the instantiation and configuration information in the design, establishes signal connectivity, and computes initial values for all objects in the design. This design hierarchy is stored in a simulation snapshot. The snapshot is the representation of your design that the simulator uses to run the simulation.

To elaborate the design:

♦ Click the plus sign to the left of the *worklib* library in the Library Browser to expand it.

♦ Expand the *xorgate* design unit (see Figure 2).

♦ Select the top-level design unit: worklib.xorgate:syn.

♦(NCL) Tools > Elaborator

D. Creating the testbench design *xorgate_test*

Repeat the step B and C to compile and elaborate xorgate_test

```
--start of vhdl code xorgate_test.vhd
LIBRARY ieee;
use ieee.std_logic_1164.all;
Entity xorgate_test IS
   END xorgate_test;
ARCHITECTURE test of xorgate_test IS
   component xorgate
         port( A, B: in std_logic;
               F: out std_logic);
   end component;
for U1: xorgate use entity work.xorgate(syn);
signal inA,inB,outF : std_logic;
BEGIN
U1: xorgate  port map(inA, inB, outF);
inA<= '1',
   '0' after 50 ns,
   '1' after 100 ns;
inB<= '0',
   '1' after 25 ns,
   '0' after 53 ns,
   '1' after 90 ns,
   '0' after 120 ns;
END test;
```

E. Simulation with NcSim

1. Loading the Snapshot into the Simulator

- ♦(NCL)Design Area, in the snapshot folder, select **worklib.xorgate_test:test** (see Figure 2).
- ♦ (NCL)Tools > Simulator

The simulator window(NCVHDL window) will show up:

2. Viewing Signals in SignalScan Waveform Viewer

You will now select signals that you want to probe to a database and display in the Signalscan waves waveform viewer. Select your design in your SimVision window: WORKLIB:XORGATE_TEST(TEST), (see Figure 3).

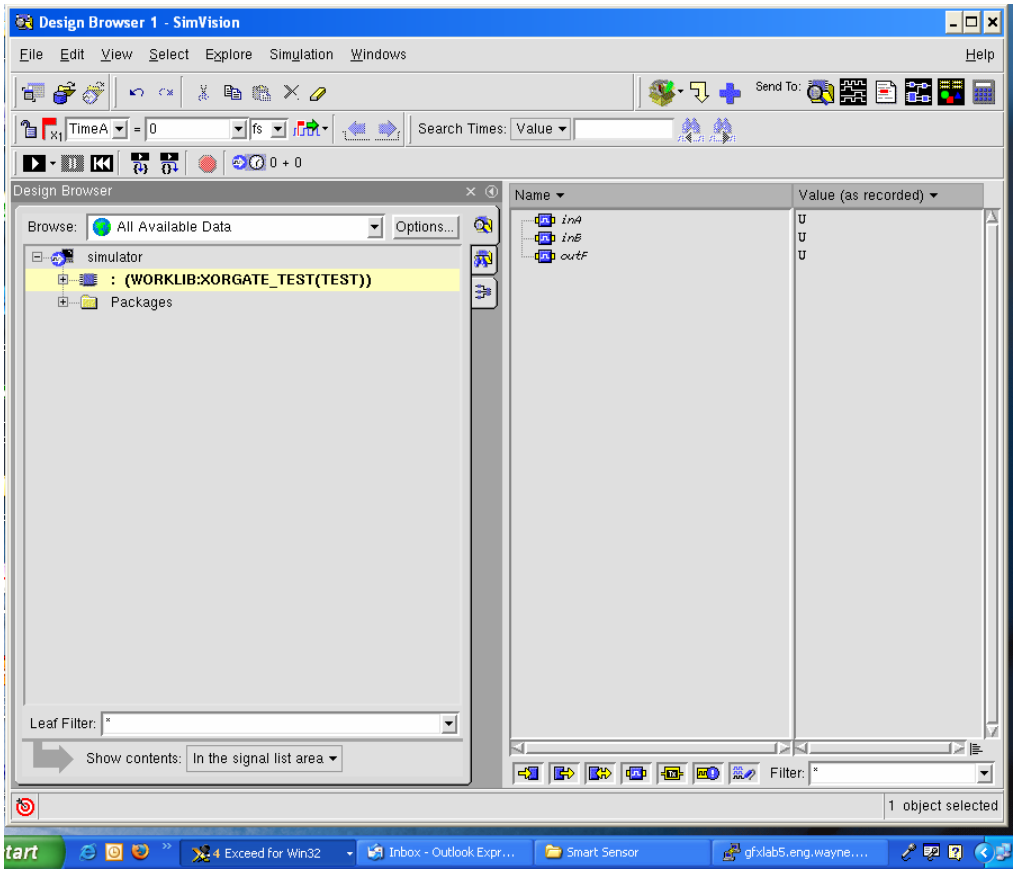


Figure 3. SimVision Window

(Simvision)Select > Signals from the menu of the simulator.

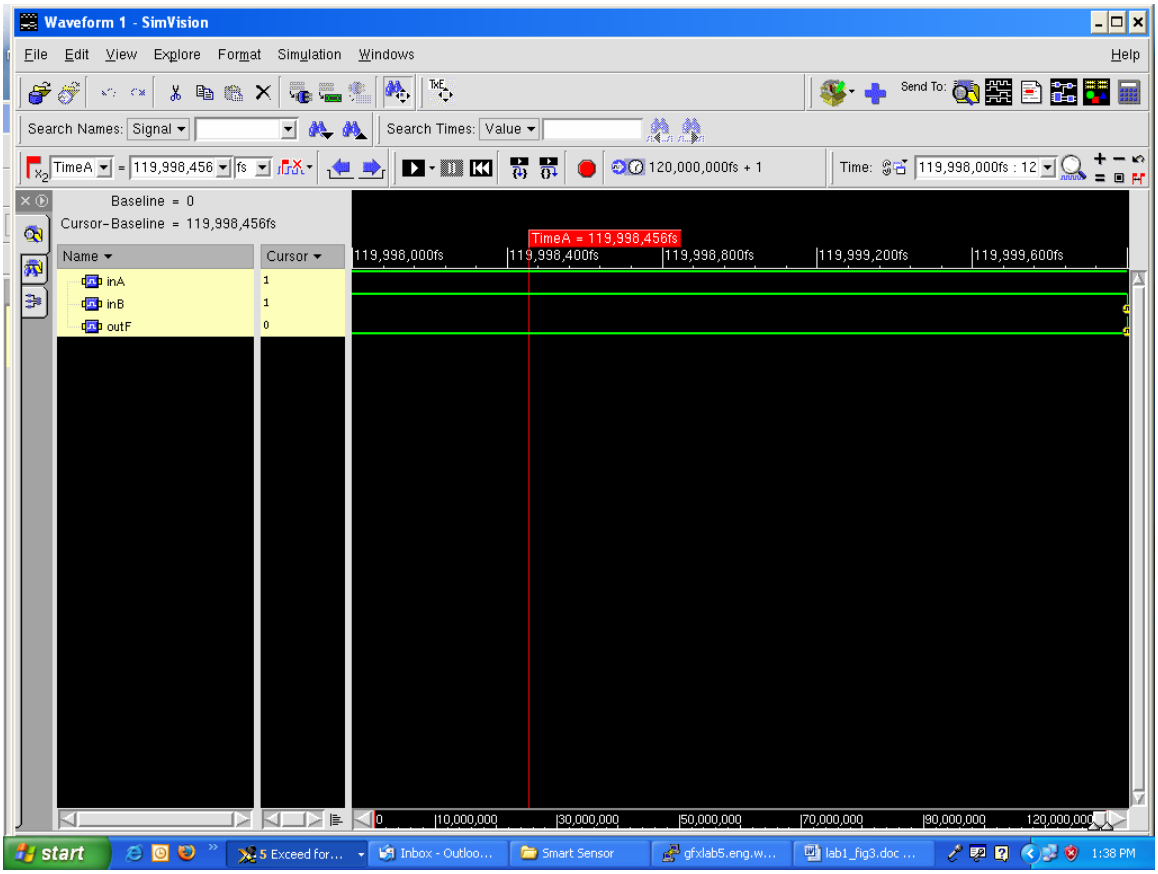
To invoke the Signal scan click on the button  in the upper right corner(**SimVison** window).

3.Simulate the design

To simulate, click the *Run Simulation* button  on the NCVHDL window or

(**Simvision**)> Run>Continue

This is the initial output of the waveform. The time axis is incorrect and must be modified to range from 0ns to 120 ns.



To edit the time axis click on the time drop box in the upper right corner and select Edit time ranges… (see Figure 7)

First select the time unit from fs to ns, this is done by clicking the

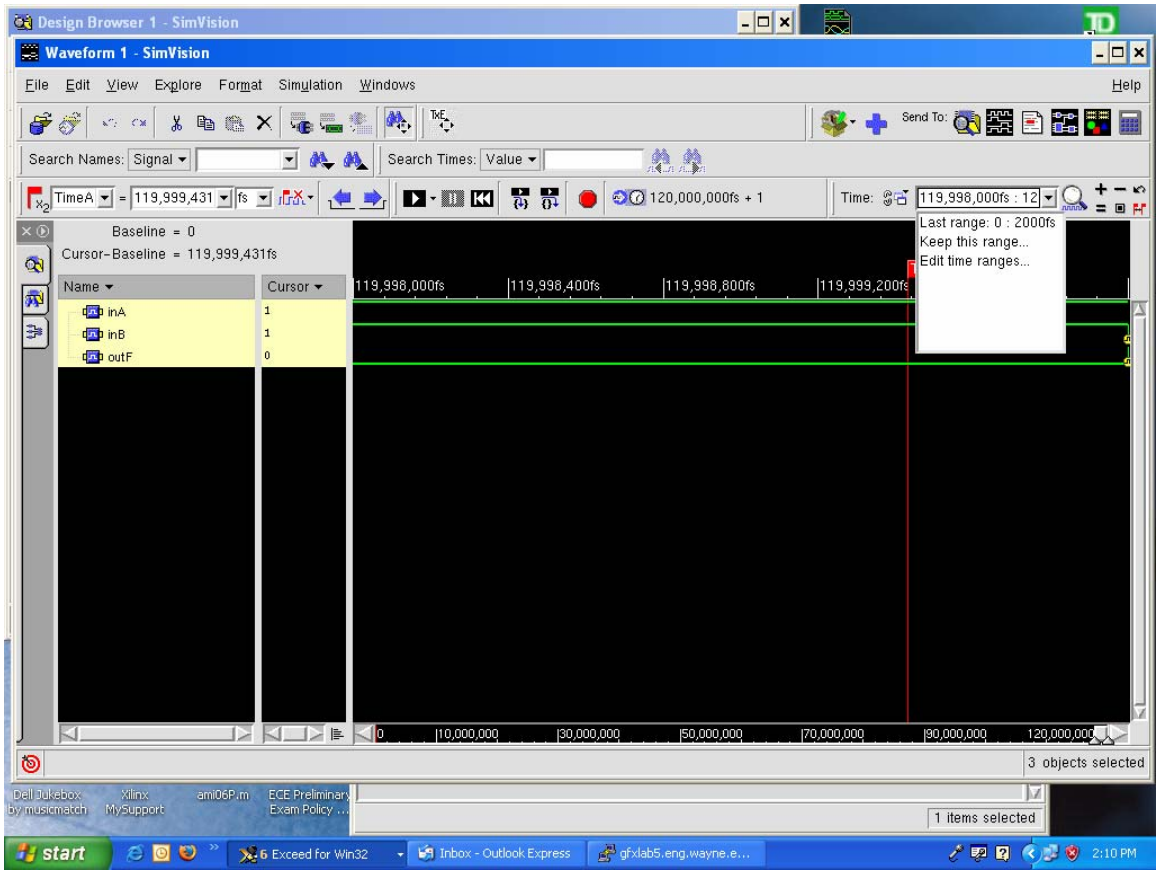


Figure 7.

The Time range editing window will display with three columns Name, Start Time, End Time.

To edit click *Create a new time range* icon in the upper left corner, see Figure 8.

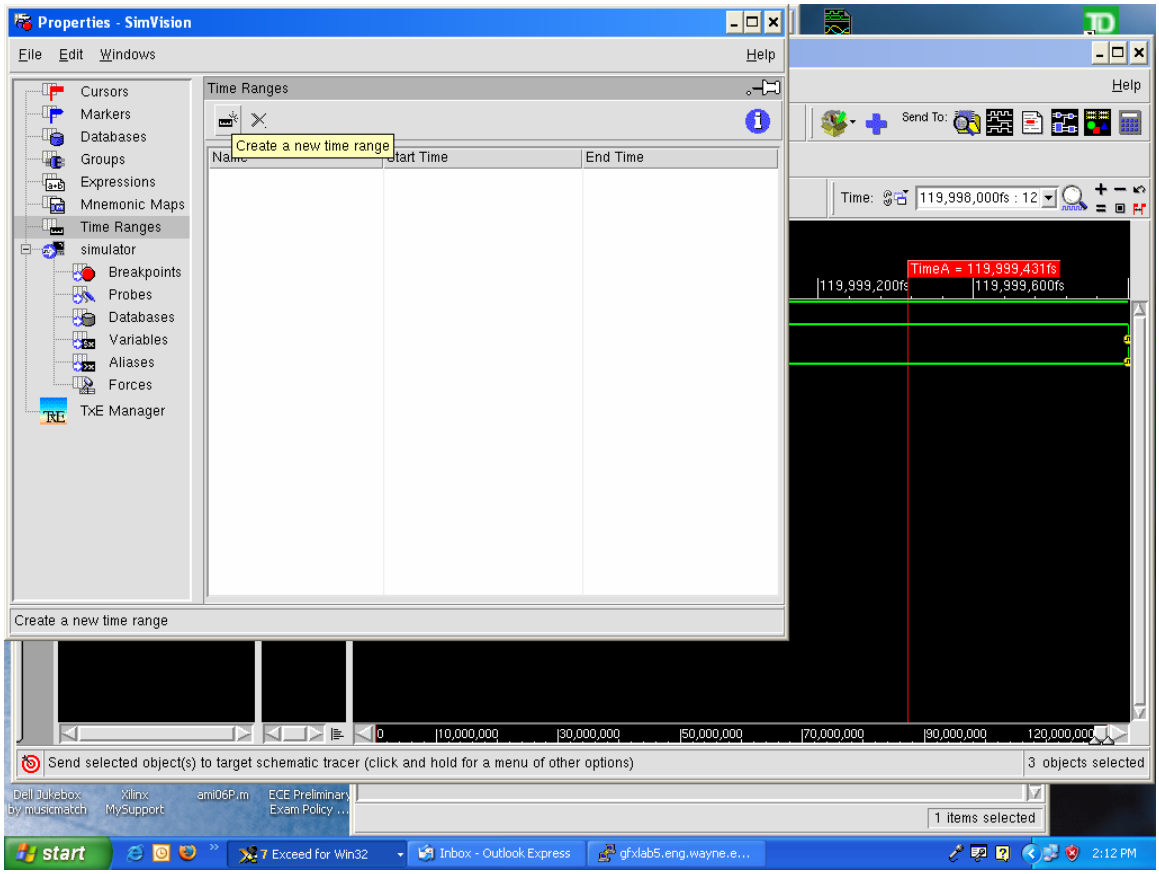
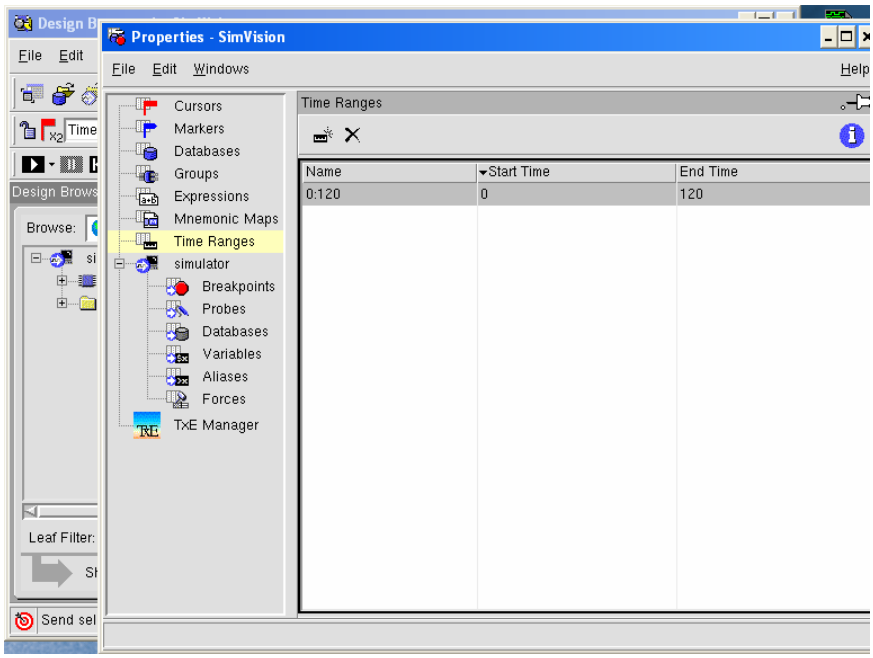


Figure 8.

To edit, click the column to edit and enter the value shown in Figure 9.



Select the newly edited time range 0:120ns, to display the correct simulated results, see Figure 10.

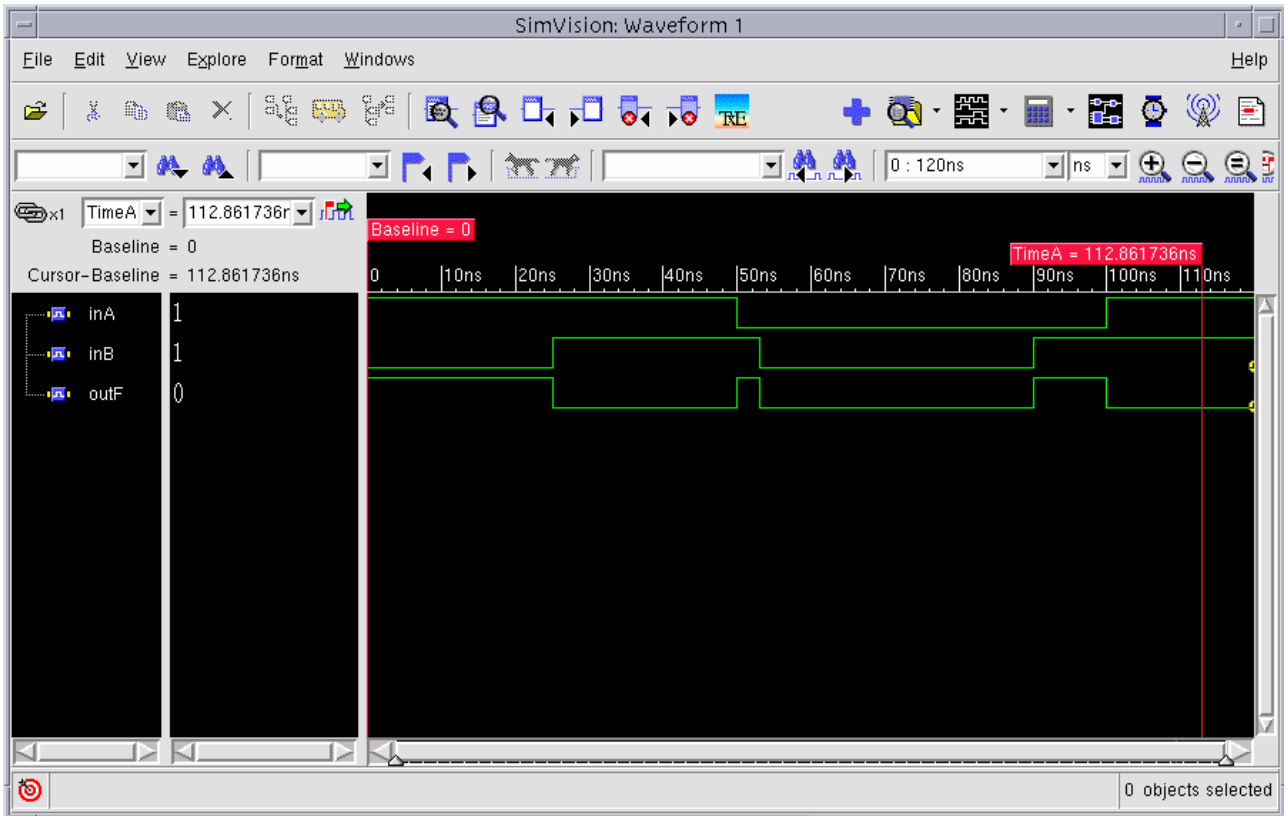


Figure 10..