No: ECE 6570/BME 6470/PHY 6570

Title: Smart Sensor Technology I: Design

Credits 4

WSU Catalog Discription:
Prereq: B.S. degree in engineering or science. Introduction to various types of sensors and the design of basic analog VLSI circuit building blocks.

Sensor Portion: Weeks 1-7

9/7/05-10/21/05
Coordinator: Gregory Auner, Professor of Electrical and Computer Engineering
Instructors: Dr. Jagdish Thakur
Office hours: Wednesdays & Fridays 2:30 - 3:30 pm
Office: 3164 Engineering Building
Phone: 313-577-3788, Email: jagdish@wayne.edu

Lecture Meeting Time & Location:
Location: 2409 Engineering Bldg, Multi-Media Room
Time: 3:30-5:20, Wednesday and Friday

VLSI Portion: Weeks 8-16

10/26/05-12/14/05
Website: http://webpages.eng.wayne.edu/~cadence

Coordinator: Pepe Siy, Professor of Electrical and Computer Engineering
Instructor: Pepe Siy, Professor of Electrical and Computer Engineering
Office hours: Wednesdays & Fridays 2:30 - 3:30 pm
Office: 3125 Engineering Building
Phone: 313-577-3841, Email: psiy@ece.eng.wayne.edu

TA: Zhen Yang, Ph.D. student
Office hours: Thu 2:30 - 3:30 pm, Fri 12:30-1:30pm
Office: 3355 Engineering Building
Phone: 248-890-9001, Email: ae6876@wayne.edu
Lecture Meeting Time & Location:
Location: 2409 Engineering Bldg, Multi-Media Room
Time: 3:30-5:20, Wednesday

Lab Meeting Time & Location:
Location: Unix lab, 2nd floor Engineering Bldg
Time: 3:30-5:20PM, Thursday
1:30-3:20PM, 3:30-5:20PM, Friday
Goals: This course is divided into two main categories—(1) theoretical understanding of various physical phenomenon behind the operation of different types of sensors, (2) designing of sensors with appropriate electronic interface using VLSI technology. Various types of sensors discussed during this course are magnetic, optical, bio, chemical, radiation, electrical and mechanical etc. In general the students are introduced to the current technology of sensors: electronic, photonic, and new materials. The emphasis of integration of electronics with sensors to provides a smart transducer with an application-specific IC is also widely discussed.
Learning Objectives: At the end of this course, students will be able to:

1. Select the right sensor for a given application.
2. Design basic analog VLSI circuit building blocks.
3. Simulate, synthesize, and layout a complete VLSI chip ready for fabrication, using CADENCE CAD tools.

Textbook or Manual: Handouts posted on the Web

Reference Text: none

Prerequisites by Topic: none
Corequisites by Topic: none

Topics:

<table>
<thead>
<tr>
<th>Week</th>
<th>Date</th>
<th>TOPIC</th>
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<tbody>
<tr>
<td>1</td>
<td>9/7/05</td>
<td>Principles of Sensing, Classification and Terminology of Sensors,</td>
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<td>Measurands. Some basic discussion about electric field, potential,</td>
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<td>capacitance, resistance etc.</td>
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<td>2</td>
<td>9/14/05</td>
<td>Acoustic and Magnetic Sensors</td>
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<td>3</td>
<td>9/21/05</td>
<td>Mechanical Sensors</td>
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<td>4</td>
<td>9/28/05</td>
<td>Radiation and Thermal Sensors</td>
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<td>5</td>
<td>10/5/05</td>
<td>Chemical and Biosensors</td>
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<td>6</td>
<td>10/12/05</td>
<td>Electronic Interface and Integrated Sensors/Design Projects</td>
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<tr>
<td>7</td>
<td>10/19/05</td>
<td>Sensor and Electronic Design Projects, In class Exam (10/21/05)</td>
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<td>8</td>
<td>10/26/05</td>
<td>(Lec) Electronics interfacing overview and SCMOS technology design</td>
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<td>rule; (Lab 1) Schematic Capture Using Virtuoso Schematic Editor,</td>
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<td>(Lab 2) Functional Simulation Using: Affirma Analog Simulator.</td>
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<td>9</td>
<td>11/2/05</td>
<td>(Lec) Transistor, resistor, and capacitor standard cell layout; (Lab</td>
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<td>3) Layout Using Virtuoso Layout XL</td>
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<td>10</td>
<td>11/9/05</td>
<td>(Lec) Transmission Gate and Digital Circuit Design; (Lab 4)IC</td>
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<td>Extraction and Post Layout Simulation</td>
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<td>11</td>
<td>11/16/05</td>
<td>(Lec) Current Source/Sink &amp; Biasing Principle; (Lab 5) Hierarchical</td>
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<tr>
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<td>Designs</td>
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<tr>
<td>12</td>
<td>11/23/05</td>
<td>(Lec) Common Source Amplifier ; (Lab 6) Complete Layout with</td>
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<td>Padframe</td>
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<tr>
<td>13</td>
<td>11/30/05</td>
<td>(Lec) CMOS Inverter ; (No Lab) Project Announcement</td>
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<tr>
<td>14</td>
<td>12/7/05</td>
<td>(Lec) Common Gate and Cascode Amplifier; (Open Lab: Proj)</td>
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Assessment Methods:

**Sensor Portion: Weeks 1-7**
Midterm Exam: Exam will cover material from weeks 1-6 (25%) will take place on Friday, Oct. 21st during class.

Group Project: Presentation and report on 19th Oct (Wednesday) in room 2409 (25%)

**VLSI Portion: Weeks 8-15**
Group Project: Report Due, Dec 19, Monday on or before 5PM. (Cadence)(20%)

Individual Take Home Exam: Due, Dec 19, Monday on or before 5PM. (Pspice)(30%)

**Grading Scale:**

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<thead>
<tr>
<th>Grade</th>
<th>A</th>
<th>A-</th>
<th>B+</th>
<th>B</th>
<th>B-</th>
<th>C+</th>
<th>C</th>
<th>F</th>
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<tbody>
<tr>
<td>Score</td>
<td>&gt;=95</td>
<td>&gt;=90</td>
<td>&gt;=85</td>
<td>&gt;=80</td>
<td>&gt;=75</td>
<td>&gt;=70</td>
<td>&gt;=60</td>
<td>&lt;60</td>
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Deferred Grades A grade of "I" will only be assigned if a student IS NOT currently failing the course and if there is NOT a substantial amount of work to be completed. An "I" grade MUST be made up within one year of assignment of the grade. Assignment of an “I” grade will be at the sole discretion of the instructor.

Attendance: You will be expected to attend class and participate in discussions regarding lectures by the instructor and your classmates. In order to do this, you should read the papers given to you prior to attending class. This will include handouts and reference lists or review articles as well as the papers written by your classmates.

Blackboard Blackboard will be used throughout the course for communication among students and with the instructor. Feel free to post both private and common questions. Written assignments will be turned in and distributed to other students via Blackboard. In order to use the system, you must log on through PipeLine. Please activate your Wayne email address, forwarding it to your standard email if you wish. This will be the address with which the class communicates with you.

Withdrawal Policy The last day to drop any class with a tuition refund is the end of the second week of classes. The last day to withdraw from the class, without a notation of W on the transcript, is the end of the fourth week of classes. All drop/add activity during the first 4 weeks should be done through Pipeline. Between the end of the fourth and fifth weeks, withdrawals require the permission of the instructor and must be submitted on a Drop/Add form to the Registrar’s Office.
SYLLABUS
Smart Sensors Technology I - College of Engineering - Fall 2005

It is the policy of the College of Engineering not to allow withdrawals from courses after the end of the 5th week except under exceptional circumstances. Failing a class is not an acceptable excuse for withdrawal after the 5th week. Withdrawals after this time require the permission of the Associate Dean for Academic Affairs.

Policy on Cheating  It is the policy of the Electrical and Computer, Biomedical Engineering Programs that any instance of cheating will result in a grade of F for the course. Cheating is defined by the University as “intentionally using or attempting to use, or intentionally providing or attempting to provide, unauthorized materials, information, or assistance in any academic exercise.” This includes any group efforts on assignments or exams unless specifically approved by the professor for that assignment/exam. Evidence of fabrication or plagiarism, as defined by the University in its brochure Academic Integrity, will also result in downgrading for the course. Please refer to the “Expectations for Citation in Biomedical Engineering” handout (attached and available on the web) and to the Departmental recommended book on scientific writing, for guidance.

STUDENTS WHO CHEAT ON ANY ASSIGNMENT OR DURING ANY EXAMINATION WILL BE ASSIGNED A FAILING GRADE FOR THE COURSE.

Therefore avoid all appearance of improper behavior! Students who witness cheating should report the incident to the instructor as soon as possible. Students are also welcome to discuss any concerns related to cheating with the instructor.

“Academic dishonesty ... tends to compromise the academic integrity of the institution or subvert the education process. All forms of academic dishonesty are prohibited at Wayne State University, as outlined in the Student Due Process Policy.” -- from Academic Integrity: Important Information for Faculty and Students

Outcome Coverage:

(a) An ability to apply knowledge of mathematics, science, and engineering. The laboratory exercises and projects require knowledge of mathematics, science, and engineering to successfully complete them.

(b) An ability to design and conduct experiments, as well as to analyze and interpret data. Students are assigned both individual and group projects, which require ability to conduct simulation, analyze and interpret results.

(c) An ability to design a system, component, or process to meet desired needs within realistic constraints such as economic, environmental, social, political, ethical, health and safety, manufacturability, and sustainability. Students learn the process of VLSI chip fabrication through MOSIS. The chips are designed to achieve design specifications. Also, students learn clean room facilities to fabricate sensors for their projects.

(d) An ability to function on multi-disciplinary teams. Students work in multi-disciplinary type projects. The student’s population in the class is from different disciplines: Physics, Biomedical, Mechanical, and Electrical.

(e) An ability to identify, formulate, and solve engineering problems. Students are presented with engineering problems, like designing sensors for biomedical, automotive applications.
(g) An ability to communicate effectively. Students are required to write and present projects assigned to their group.

(i) A recognition of the need for, and an ability to engage in life-long learning. Students are exposed to multi-disciplinary type of projects requiring continuous and life-long learning. The students need to learn new discipline to conduct and complete projects.

(k) An ability to use the techniques, skills, and modern engineering tools necessary for engineering practice. Students learn the skills in creating VLSI layout using state of the art CAD tools (CADENCE software package). Learned electronic circuits simulation using SPICE.