Cascode Amplifier

Figure 1(a) shows a cascode amplifier with ideal current source load. Figure 1(b) shows the ideal current source is implemented by PMOS with constant gate to source voltage.

\[ V_{DD} - (|V_{TP0}| + |\Delta V|) = V_{G3} \]
\[ V_{DD} - (|V_{TP0}| + |\Delta V|) = V_{G3} = V_{G2} - \Delta V \]
\[ V_{TN0} + V_{TN2} + 2\Delta V = V_{G2} \]
\[ V_{TN0} + \Delta V = V_{i} \]
\[ V_{SS} = 0 \]

Figure 1. Cascode amplifier with simple current load.

1. Low Frequency Small Signal Equivalent Circuit

Figure 2(a) and 2(b) show its low frequency small signal equivalent circuit. Figure 2( c) shows its two-port representation and port variables assignment.
Figure 2. Cascode amplifier low frequency small signal equivalent circuit.
The current equation of network a is:

\[ I_1^a = 0 \]
\[ I_2^a = g_{m1} V_1^a + g_{ds1} V_2^a \]

The corresponding Y-parameter matrix is:
\[ Y^a = \begin{bmatrix} 0 & 0 \\ g_{m1} & g_{ds1} \end{bmatrix} \]

The current equation of network b is:

\[ I_1^b = (g_{m2} + g_{mb2} + g_{ds2}) V_1^b - g_{ds2} V_2^b \]
\[ I_2^b = -(g_{m2} + g_{mb2} + g_{ds2}) V_1^b + g_{ds2} V_2^b \]

The corresponding Y-parameter matrix is:
\[ Y^b = \begin{bmatrix} g_{m2} + g_{mb2} + g_{ds2} & -g_{ds2} \\ -(g_{m2} + g_{mb2} + g_{ds2}) & g_{ds2} \end{bmatrix} \]

The common gate stage gain is:
\[ A_V^b = \frac{Y_{21}^b}{Y_{22}^b + Y_L^b} = \frac{g_{m2} + g_{mb2} + g_{ds2}}{g_{ds2} + g_{ds3}} \]

The input impedance of common gate stage (the load of common source stage) is:
\[ Z_i^b = Z_L^b = \frac{Y_{22}^b + Y_L^b}{\text{det}Y^b + Y_{11}^b Y_L^b} = \frac{g_{ds2} + g_{ds3}}{(g_{m2} + g_{mb2} + g_{ds2}) g_{ds3}} \approx \frac{2}{g_{m2}} \]

The gain of the common source stage is:
\[ A_V^a = \frac{-Y_{21}^a}{Y_{22}^a + Y_L^a} = \frac{-g_{m1}}{g_{ds1} + (g_{m2} + g_{mb2} + g_{ds2}) g_{ds3} + g_{ds2} g_{ds3}} \approx \frac{-g_{m1} (g_{ds2} + g_{ds3})}{g_{ds1} (g_{ds2} + g_{ds3}) + (g_{m2} + g_{mb2} + g_{ds2}) g_{ds3}} \approx \frac{-2g_{m1}}{g_{m2} + g_{mb2}} \approx 2 \]

Assuming all \( g_m \) are equal, and all \( g_{ds} \) are equal. In addition \( g_m >> g_{mb} \) and \( g_m >> g_{ds} \).

With a gain of 2 the miller capacitance \( C_{gd1} \) of the common source stage is negligible.
The overall gain is:

\[ A_V = A_V^a A_V^b = \left( \frac{g_{m2} + g_{mb2} + g_{dc2}}{g_{ds2} + g_{ds3}} \right) \left( \frac{-g_{m1}(g_{ds2} + g_{ds3})}{g_{ds1}g_{ds2} + g_{ds1}g_{ds3} + g_{ds2}g_{ds3} + (g_{m2} + g_{mb2})g_{ds3}} \right) \]

\[ = \frac{-g_{m1}(g_{m2} + g_{mb2} + g_{dc2})}{g_{ds1}g_{ds2} + g_{ds1}g_{ds3} + (g_{m2} + g_{mb2} + g_{dc2})g_{ds3}} \approx \frac{-g_m}{g_{ds}} \]

The output impedance of the cascode amplifier is computed by obtaining the output impedance of the common source stage (or the source impedance of the common gate stage) first. That is,

\[ Z_o^a = Z_S^b = \frac{y_{11}^a + Y_S^a}{\text{det}Y_S^a + y_{22}^a Y_S^a} = \frac{1}{g_{ds1}} \]

The result is obtained by dividing the numerator and denominator by \( Y_S^a \). The output impedance of the cascode is the output impedance of the common gate stage.

\[ Z_o^b = \frac{y_{11}^b + Y_S^b}{\text{det}Y_S^b + y_{22}^b Y_S^b} = \frac{g_{m2} + g_{mb2} + g_{dc2} + g_{dl1}}{g_{ds2}g_{ds1}} = (g_{m2} + g_{mb2})r_{ds2}r_{ds1} + r_{ds1} + r_{ds2} \approx g_{m2}r_{ds2}r_{ds1} \]

That is, the output impedance is equal to the output impedance, \( r_{ds1} \), of the first stage (common source) magnified by the gain, \( g_{m2}r_{ds2} \), of the second stage (common gate). The effective load is the parallel combination of output impedance of the cascode amplifier and the load.

\[ Z_o = Z_o^b // Z_L = ((g_{m2} + g_{mb2})r_{ds2}r_{ds1} + r_{ds1} + r_{ds2}) // r_{ds3} \approx (g_{m2}r_{ds2}r_{ds1})//r_{ds3} \approx r_{ds3} \]

The overall gain is approximately equal to:

\[ A_V = -g_{m1}Z_o \approx -g_{m1}r_{ds3} \]

Although the output impedance has been magnified but the effective load impedance is determined by smaller impedance. That is, \( r_{ds3} \).

The overall gain of the cascode amplifier can be increased if we can increased \( r_{ds3} \). This can be achieved by adding a cascode at the load. This is shown in Figure 3. Figure 4 shows its low frequency small signal equivalent circuit and its two-port representations and port variables assignment. There are three two-port networks. The Y-parameter matrices are derived as follows:

The current equation of network a is:

\[ I_1^a = 0 \]

\[ I_2^a = g_{m1} V_1^a + g_{ds1} V_2^a \]

The corresponding Y-parameter matrix is:
The current equation of network b is:

\[ I_1^{b} = (g_{m2} + g_{mb2} + g_{ds2})V_1^{b} - g_{ds2}V_2^{b} \]
\[ I_2^{b} = -(g_{m2} + g_{mb2} + g_{ds2})V_1^{b} + g_{ds2}V_2^{b} \]

The corresponding Y-parameter matrix is:

\[
Y^{b} = \begin{bmatrix}
g_{m2} + g_{mb2} + g_{ds2} & -g_{ds2} \\
-(g_{m2} + g_{mb2} + g_{ds2}) & g_{ds2}
\end{bmatrix}
\]

The current equation of network c is:

\[ I_1^{c} = (g_{m3} + g_{mb3} + g_{ds3})V_1^{c} - g_{ds3}V_2^{c} \]
\[ I_2^{c} = -(g_{m3} + g_{mb3} + g_{ds3})V_1^{c} + g_{ds3}V_2^{c} \]

The corresponding Y-parameter matrix is:

\[
Y^{c} = \begin{bmatrix}
g_{m3} + g_{mb3} + g_{ds3} & -g_{ds3} \\
-(g_{m3} + g_{mb3} + g_{ds3}) & g_{ds3}
\end{bmatrix}
\]

The output impedance of network b has been obtained earlier it is,

\[ Z_{o}^{b} = (g_{m2} + g_{mb2})r_{ds2}r_{ds1} + r_{ds1} + r_{ds2} \approx g_{m2}r_{ds2}r_{ds1} \]

The output impedance of network c is computed as follows:

\[ Z_{o}^{c} = \frac{Y_{11}^{c} + Y_{22}^{c}}{\det Y^{c}} \approx \frac{g_{ds3}g_{ds4}}{g_{ds3}g_{ds4}} = (g_{m3} + g_{mb3})r_{ds3}r_{ds4} + r_{ds3} + r_{ds4} \approx g_{m3}r_{ds3}r_{ds4} \]

The effective load impedance is the parallel combination of the output impedance of network b and c.

\[ Z_{o} = Z_{o}^{b} / Z_{o}^{c} \approx \frac{g_{m}r_{ds}^2}{2} \]

Assuming all \( g_{m} \) are equal and all \( g_{ds} \) are equal.
Figure 3. Cascode amplifier with cascode current load.
Figure 4. Cascode amplifier with cascode load low frequency small signal equivalent circuit.
2. High Frequency Small Signal Equivalent Circuit

![Cascode amplifier parasitic capacitances](image)

Figure 5. Cascode amplifier parasitic capacitances.

Figure 5 shows all the parasitic capacitances needed for high frequency modelling. Figure 6(a) shows the high frequency small signal equivalent circuit of cascode amplifier with simple current load. Figure 6(b) its two-port representation and port variables assignment.

\[ Y_L = Y_L^h = g_{ds3} + sC_3; \quad Y_S = \infty \text{ (or } Z_S = 0) \]

\[ C_1 = C_{gd1}; \quad C_2 = C_{db1} + C_{gs2} + C_{sb2}; \quad C_3 = C_{gd2} + C_{db2} + C_{db3} + C_{gd3} + C_L \]

The input capacitance \( C_{gs1} \) is assumed to be part of the input voltage source. \( C_{gs3} \) is shorted out by the input voltage source, it does not affect the circuit operation, hence can be ignored or deleted. \( C_3 \) is assumed to be part of the load. The current of the first stage (network a) is given by:

\[ I_1^a = sC_1V_1^2 - sC_1V_2^2 \]

\[ I_2^a = (g_{m1} - sC_1)V_1^2 + [g_{ds1} + s(C_1 + C_2)]V_2^2 \]
The current equation of network \( b \) is:

\[
\begin{align*}
\mathbf{Y}^a &= \begin{bmatrix}
  sC_1 & -sC_1 \\
g_m - sC_1 & [g_{ds1} + s(C_1 + C_2)]
\end{bmatrix} \\
\mathbf{Y}^b &= \begin{bmatrix}
  I_{2a} & I_{1b} \\
V_{2a} & V_{1b}
\end{bmatrix} \\
Z_{1b} &= \begin{bmatrix}
  I_{2b} \\
V_{2b}
\end{bmatrix} \\
Z_{0b} &= \begin{bmatrix}
  G_L \\
0
\end{bmatrix}
\end{align*}
\]

Figure 6. Cascode amplifier high frequency equivalent circuit.
\( I_i^b = (g_{m2} + g_{mb2} + g_{ds2})V_1^a - g_{ds2}V_2^a \)

\( I_2^b = -(g_{m2} + g_{mb2} + g_{ds2})V_1^a + g_{ds2}V_2^a \)

The corresponding \( Y \)-parameter matrix is:

\[
Y^b = \begin{bmatrix}
g_{m2} + g_{mb2} + g_{ds2} & -g_{ds2} \\
-(g_{m2} + g_{mb2} + g_{ds2}) & g_{ds2}
\end{bmatrix}
\]

The voltage gain of network \( b \) is:

\[
A_V^b = \frac{-y_{21}^b}{y_{22}^b + \frac{Y^b}{Y_L^b}} = \frac{g_{ds2} + g_{ds3} + sC_3}{g_{ds2} + g_{ds3} + sC_3}
\]

The input impedance of network \( b \) or load of network \( a \) is:

\[
Z_i^b = Z_L^b = \frac{y_{22}^b + \frac{Y^b}{Y_L^b}}{\det Y^b + \frac{Y^b}{Y_L^b}} = \frac{g_{ds2} + g_{ds3} + sC_3}{(g_{m2} + g_{mb2} + g_{ds2})(g_{ds3} + sC_3)}
\]

The voltage gain of network \( a \) is:

\[
A_V^a = \frac{-y_{21}^a}{y_{22}^a + \frac{Y^a}{Y_L^a}} = \frac{- (g_{m1} - sC_1)}{g_{ds1} + s(C_1 + C_2) + \frac{(g_{m2} + g_{mb2} + g_{ds2})(g_{ds3} + sC_3)}{g_{ds2} + g_{ds3} + sC_3}}
\]

\[
= \frac{(g_{m1} - sC_1)(g_{ds2} + g_{ds3} + sC_3)}{(g_{ds1} + s(C_1 + C_2))(g_{ds2} + g_{ds3} + sC_3) + (g_{m2} + g_{mb2} + g_{ds2})(g_{ds3} + sC_3)}
\]

The overall gain of the cascode amplifier is:
$$A_V = A_V^b A_V^a$$
$$= \frac{g_{m2} + g_{mb2} + g_{ds2}}{g_{ds2} + g_{ds1} + sC_3} \left( \frac{-(g_{m1} - sC_1)(g_{ds2} + g_{ds3} + sC_3)}{(g_{ds1} + s(C_1 + C_2))(g_{ds2} + g_{ds3} + sC_3) + (g_{m2} + g_{mb2} + g_{ds2})(g_{ds3} + sC_3)} \right)$$
$$= \frac{-(g_{m1} - sC_1)(g_{m2} + g_{mb2} + g_{ds2})}{(g_{ds1} + s(C_1 + C_2))(g_{ds2} + g_{ds3} + sC_3) + (g_{m2} + g_{mb2} + g_{ds2})(g_{ds3} + sC_3)}$$
$$= \frac{- (g_{m1} - sC_1)(g_{m2} + g_{mb2} + g_{ds2})}{c[1 + bs + as^2]}$$

where:

$$a = \frac{C_3(C_1 + C_2)}{g_{ds1}g_{ds2} + g_{ds3}(g_{m2} + g_{mb2} + g_{ds1} + g_{ds2})}$$

$$b = \frac{C_3(g_{ds1} + g_{ds2} + g_{m2} + g_{mb2}) + C_2(g_{ds2} + g_{ds3}) + C_1(g_{ds2} + g_{ds3})}{g_{ds1}g_{ds2} + g_{ds3}(g_{m2} + g_{mb2} + g_{ds1} + g_{ds2})}$$

$$c = g_{ds1}g_{ds2} + g_{ds3}(g_{m2} + g_{mb2} + g_{ds1} + g_{ds2})$$

If the poles are far apart, it can be approximated as follows:

$$D(s) = 1 + bs + as^2 = \left( 1 - \frac{s}{p_1} \right) \left( 1 - \frac{s}{p_2} \right) = 1 - \left( \frac{1}{p_1} + \frac{1}{p_2} \right)s + \left( \frac{1}{p_1 p_2} \right)s^2 \approx 1 - \left( \frac{1}{p_1} \right)s + \left( \frac{1}{p_1 p_2} \right)s^2$$

where: $$|p_2| >> |p_1|$$

That is,

$$p_1 = -\frac{1}{b} \approx -\frac{-g_{ds1}g_{ds2} + g_{ds3}(g_{m2} + g_{mb2} + g_{ds1} + g_{ds2})}{C_3(g_{ds1} + g_{ds2} + g_{m2} + g_{mb2}) + C_2(g_{ds2} + g_{ds3}) + C_1(g_{ds2} + g_{ds3})} \approx -\frac{g_{ds3}}{C_3}$$

$$p_2 = -\frac{b}{a} \approx -\frac{-[C_3(g_{ds1} + g_{ds2} + g_{m2} + g_{mb2}) + C_2(g_{ds2} + g_{ds3}) + C_1(g_{ds2} + g_{ds3})]}{C_3(C_1 + C_2)} \approx -\frac{g_{m2}}{C_1 + C_2}$$

Note that the poles are associated with the inverse product of the resistance and capacitance of a node to ground. $$p_1$$ is associated with node D2 to ground, and $$p_2$$ is associated with D1 (or S2) to ground. The cascode amplifier also has a zero at the right half plane given by:

$$z_1 = \frac{g_{m1}}{C_1}$$
3. Cascode Amplifier with Simple Current Load

The biasing voltages will be determined by ignoring the effect of the bulk voltage on M2. Using the biasing principle discussed in the current sink/source section. The biasing requirement from Figure 1(b) are:

\[ V_{bias} = V_{TN0} + \Delta V = 1 + 1.5 = 2.5 \]
\[ V_{G2} = 2V_{TN} + 2\Delta V = 2(1) + 2(1.5) = 5 \]
\[ V_{G3} = V_{DD} - (|V_{TP0}| + |\Delta V|) = V_{DD} - (| -1 | + | 1.5 |) = V_{DD} - 2.5 \]

The output voltage dynamic range with the above biasing is:

\[ V_{TN} + 2\Delta V \leq V_O \leq V_{DD} - \Delta V \]
\[ 1 + 2(1.5) = 4 \leq V_O \leq V_{DD} - 1.5 \]
\[ 4 \leq V_O \leq 6; \text{ If } V_{DD} = 7.5 \]
\[ V_{G3} = V_{DD} - 2.5 = 7.5 - 2.5 = 5 \]

The effect of bulk bias on M2 on the output voltage will be considered next. The actual minimum output voltage will be determined. The threshold voltage of M2 is no longer equal to \( V_{T0} \), due to the present of the bulk bias.

\[ V_{BS2} = -V_{DS1} \]
\[ V_{TN2} = V_{TN0} + \gamma(\sqrt{\phi - V_{BS2}} - \sqrt{\phi}) = V_{TN0} + \gamma(\sqrt{\phi + V_{DS1}} - \sqrt{\phi}) \]
\[ V_{DS1} = V_{G2} - V_{TN2} - \Delta V \]
\[ V_{TN2} = V_{T0} + \gamma(\sqrt{\phi + V_{G2} - V_{TN2} - \Delta V} - \sqrt{\phi}) \]

Solve for \( V_{TN2} \) by iteration

\[ V_{TN2} = 1.75 \]
\[ V_{DS1(\min)} = V_{G2} - V_{TN2} - \Delta V = 5 - 1.75 - 1.5 = 1.75 \]
\[ V_{DS2(\min)} = \Delta V = 1.5 \]
\[ V_{O(\min)} = V_{DS1(\min)} + V_{DS2(\min)} = 1.75 + 1.5 = 3.25 \]
\[ 3.325 \leq V_O \leq 6 \]

The bulk bias increases the output voltage dynamic range. Using the above biasing voltages, Pspice simulation is conducted to obtain the DC transfer characteristic curve. The Pspice netlist below is used to obtain the DC transfer characteristic.
*PSpice file for NMOS Common Gate Amplifier with
*PMOS Current Load
*Filename="Lab3.cir"
VIN 1 0 DC 2.5212VOLT AC 1V
VDD 3 0 DC 7.5VOLT
VSS 4 0 DC 0VOLT
VG2 6 0 DC 5VOLT
VG3 7 0 DC 5VOLT
M1 5 1 4 4 MN W=9.6U L=5.4U
M2 2 6 5 4 MN W=9.6U L=5.4U
M3 2 7 3 3 MP W=25.8U L=5.4U

.MODEL MN NMOS VTO=1 KP=40U
+ GAMMA=1.0 LAMBDA=0.02 PHI=0.6
+ TOX=0.05U LD=0.5U CJ=5E-4 CJSW=10E-10
+ U0=550 MJ=0.5 MJSW=0.5 CGSO=0.4E-9 CGDO=0.4E-9
.MODEL MP PMOS VTO=1 KP=15U
+ GAMMA=0.6 LAMBDA=0.02 PHI=0.6
+ TOX=0.05U LD=0.5U CJ=5E-4 CJSW=10E-10
+ U0=200 MJ=0.5 MJSW=0.5 CGSO=0.4E-9 CGDO=0.4E-9

*Analysis
.DC VIN 0 7.5 0.05
.TF V(2) VIN
.AC DEC 100 1HZ 10GHZ
.PROBE
.END

The exact $V_{bias}$ is determined by locating a point in the DC transfer characteristic curve with the highest slope. The AC small signal characteristic and operating node voltages are then obtained at this operating point. The Pspice node voltages at the operating point is given below:

<table>
<thead>
<tr>
<th>NODE</th>
<th>VOLTAGE</th>
</tr>
</thead>
<tbody>
<tr>
<td>(1)</td>
<td>2.5212</td>
</tr>
<tr>
<td>(2)</td>
<td>4.6987</td>
</tr>
<tr>
<td>(3)</td>
<td>7.5000</td>
</tr>
<tr>
<td>(4)</td>
<td>0.0000</td>
</tr>
<tr>
<td>(5)</td>
<td>1.7410</td>
</tr>
<tr>
<td>(6)</td>
<td>5.0000</td>
</tr>
<tr>
<td>(7)</td>
<td>5.0000</td>
</tr>
</tbody>
</table>

The voltage at node 5 is 1.7410 which is reasonably closed to the calculated value of $V_{DS1(min)}=1.75$. If we ignore the bulk bias of M2 the calculated value is:

$$V_{DS1(min)} = V_{TN0} + \Delta V = 1 + 1.5 = 2.5$$

The DC transfer characteristic curve is given below:
Theoretical calculations of the small signal parameters are given below:

\[ \beta_{N1} = K_N (W/L)_1 = (40E - 6)(9.6u/4.4u) = 87.3uA/V^2 \]
\[ I_{DSQ} = \frac{\beta_{N1}}{2}(V_{bias} - V_{SS} - V_{T0})^2 = (87.3E - 6/2)(2.5212 - 0 - 1)^2 = 101\mu A \]
\[ R_{out} = r_{ds3} = \frac{1}{\beta_{N1}} = \frac{1}{(0.02)(101E - 6)} = .495M \]
\[ g_{m1} = g_{m2} = \sqrt{2}\beta_{N1}I_{DSQ} = \sqrt{2}(87.3E - 6)(101E - 6) = 132.79\mu mho \]
\[ A_{\text{V0}} = -g_{m1}R_{out} = -(132.79E - 6)(.495E6) = -65.75 \text{ or } 36.355\text{db} \]

The Pspice results are:

\[ R_{out} = .5M \]
\[ A_{\text{V0}} = -67.95 \text{ or } 36.644\text{db} \]

**** SMALL-SIGNAL CHARACTERISTICS
\[ V(2)/V_{IN} = -6.795E+01 \]

INPUT RESISTANCE AT \( V_{IN} = 1.000E+20 \)

OUTPUT RESISTANCE AT \( V(2) = 5.000E+05 \)

4. Cascode Amplifier High Frequency Model Experiments

The parasitic capacitances will be determined to check the theory against Pspice simulation results. The capacitances are determined at the operating point. The reverse bulk bias are first calculated at the quiescent operating point.

For M1

\[ V_{BD} = V(4) - V(5) = 0 - 1.7410 = -1.7410 \]

\[ V_{BS} = 0, \text{ bulk connected to source} \]

For M2

\[ V_{BD} = V(4) - V(2) = 0 - 4.6987 = -4.6967 \]

\[ VBS = V(4) - V(5) = 0 - 1.7410 = -1.7410 \]

For M3

\[ VBD = -(V(3) - V(2)) = -(7.5 - 4.6987) = -2.8013 \]

The MATLAB program is invoked to obtain the parasitic capacitances.

For M1,

\[ [C_{GS}, C_{GD}, C_{BD}, C_{BS}] = \text{cap}(9.6, 5.4, -1.7410, 0) \]

\[ C_{GS} = 23.2704 \text{fF}, \ C_{GD} = 3.84 \text{fF}, \ C_{BD} = 24.1791 \text{fF}, \ C_{BS} = 61.84 \text{fF} \]

For M2,

\[ [C_{GS}, C_{GD}, C_{BD}, C_{BS}] = \text{cap}(9.6, 5.4, -4.6987, -1.7410) \]

\[ C_{GS} = 23.2704 \text{fF}, \ C_{GD} = 3.84 \text{fF}, \ C_{BD} = 16.0715 \text{fF}, \ C_{BS} = 38.2591 \text{fF} \]

For M3,

\[ [C_{GS}, C_{GD}, C_{BD}, C_{BS}] = \text{cap}(25.8, 5.4, -2.8013, 0) \]

\[ C_{GS} = 62.5392 \text{fF}, \ C_{GD} = 10.32 \text{fF}, \ C_{BD} = 47.956 \text{fF}, \ C_{BS} = 152.02 \text{fF} \]

In the simulation without specifying the area and perimeter of source and drain, only \( C_{GS} \) and \( C_{GD} \) are accounted in computing the parasitic capacitances. These are calculated below:

\[ C_1 = C_{gd1} = 3.84 \text{fF} \]

\[ C_2 = C_{gs2} = 23.2704 \text{fF} \]

\[ C_3 = C_{gd2} + C_{gd3} + C_L = 3.84 \text{fF} + 10.32 \text{fF} + 0 = 14.16 \text{fF} \]
In the Pspice simulation, if the PM is determined at the frequency where zero db gain occurs the result is:

\[ f_{GBW} = 1G \text{ @0db} \]

PM = 33.84

This result seems to be quite different from the theoretical result of

\[ f_{GBW} = 1.493G \]

PM = 12.19

The discrepancy occurs because the non-dominant pole \( p_2 = 4.898E9 \) occurs before the gain bandwidth product \( w_{GBW} = 9.38E9 \). The gain bandwidth calculation assumes that the slope of -20db/dec is maintain before intersecting the zero db line. With \( p_2 \) occurring before \( w_{GBW} \), means that the slope becomes -40db/dec, causing it to intersect the zero db gain line sooner. If one extend the -20db/dec line in the Pspice simulation, this line will intersect the zero db gain axis at:

\[ f_{GBW} = A_{V0}f_{BW} = (67.95)(22.496M) = 1.53G \]

If the phase margin is determined at 1.53G, the result is 16.744° which is closer to the theoretical calculation of 12.19°. That is, the
Theoretical calculation will be in error if the non-dominant pole $p_2$ occurs before $w_{3dB}$. 

![Diagram](image-url)
The PM of 33.84 is rather low. For stability a PM of at least 60 is desirable. Looking at the PM calculation, one can increase the PM by decreasing $w_{gbw}$. Increasing the value of capacitor $C_3$ will decrease $w_{gbw}$ while maintaining the value of $p_i$. $C_3$ is a function of the load capacitance $C_i$. One can compute the value of $C_i$ needed to achieve the desired PM. To illustrate this we will compute the value of $C_i$ for a PM=80.

First compute $w_{gbw}$ to achieve PM=80.

\[
PM = 90 - \tan^{-1}\left(\frac{W_{GBW}}{z}\right) - \tan^{-1}\left(\frac{W_{GBW}}{p_2}\right) = 80
\]

\[
\tan^{-1}\left(\frac{W_{GBW}}{z}\right) + \tan^{-1}\left(\frac{W_{GBW}}{p_2}\right) = 10
\]

\[
\tan^{-1}\left(\frac{W_{GBW}}{34.1E9}\right) + \tan^{-1}\left(\frac{W_{GBW}}{4.898E9}\right) = 10
\]

$w_{gbw} = 0.75G$

The value of load capacitance is then calculated to achieve $w_{gbw}$.
\[ w_{GBW} = A_v \left( \frac{1}{r_{ds} C_3} \right) \]

\[ C_3 = \frac{A_v}{r_{ds} w_{GBW}} = 14.16 \text{fF} + C_L \]

\[ C_L = \frac{A_v}{r_{ds} w_{GBW}} - 14.16 \text{fF} = \frac{67.95}{(4.95 \times 10^6)(0.75 \times 10^9)} - 14.16 \text{fF} = 183.03 \text{fF} - 14.16 \text{fF} = 168.87 \text{fF} \]

The result of Pspice simulation with \( C_L \) added shows that PM is now 82.195°.

**5. Cascode Amplifier With Cascode Current Load Experiments**

The derivation of the biasing circuit is shown in Figure 7. The complete circuit is shown in Figure 8.
Figure 7. Biasing circuit for the cascode amplifier with cascode load.
Figure 8. Complete circuit of the cascode amplifier with cascode load.

Netlist for the complete circuit of Figure 8 is shown below:

*PSpice file for NMOS Common Gate Amplifier with PMOS Current Load
*Filename="Lab32b.cir"
*All bulks are connected to supply rail
.PARAM Wn=9.6U, Ln=5.4U
.PARAM Wp=25.8U, Lp=5.4U
VIN 1 10 DC 0VOLT AC 1V
VDD 3 0 DC 10VOLT
VSS 4 0 DC 0VOLT

M1 5 1 4 4 NMOS1 W={Wn} L={Ln}
M2 2 7 5 4 NMOS1 W={Wn} L={Ln}
M3 2 8 6 3 PMOS1 W={Wp} L={Lp}
M4 6 9 3 3 PMOS1 W={Wp} L={Lp}

*Biasing circuit
MBN1 10 10 4 4 NMOS1 W={Wn} L={Ln}
MBN2 7 7 10 4 NMOS1 W={Wn} L={Ln}
IBP 8 4 100UA
MBP1 8 8 9 3 PMOS1 W={Wp} L={Lp}
MBP2 9 9 3 3 PMOS1 W={Wp} L={Lp}
MBP3 7 8 11 3 PMOS1 W={Wp} L={Lp}
MBP4 11 9 3 3 PMOS1 W={Wp} L={Lp}
.MODEL NMOS1 NMOS VTO=1 KP=40U
+ GAMMA=1.0 LAMBDA=0.02 PHI=0.6
+ TOX=0.05U LD=0.5U CJ=5E-4 CJSW=10E-10
+ U0=550 MJ=0.5 MJSW=0.5 CGSO=0.4E-9 CGDO=0.4E-9

.MODEL PMOS1 PMOS VTO=-1 KP=15U
+ GAMMA=0.6 LAMBDA=0.02 PHI=0.6
+ TOX=0.05U LD=0.5U CJ=5E-4 CJSW=10E-10
+ U0=200 MJ=0.5 MJSW=0.5 CGSO=0.4E-9 CGDO=0.4E-9

*Analysis
.DC VIN -2.5 7.5 0.05
.TF V(2) VIN
.AC DEC 100 1HZ 10GHZ
.PROBE
.END

NODE VOLTAGE NODE VOLTAGE NODE VOLTAGE NODE VOLTAGE

( 1) 2.4774 ( 2) 5.9211 ( 3) 10.0000 ( 4) 0.0000
( 5) 2.4774 ( 6) 7.5450 ( 7) 5.9211 ( 8) 4.4772
( 9) 7.5280 (10) 2.4774 (11) 7.5450
The biasing voltages are obtained from the above table

VG1=Vbias=V(10)=2.4774
VG2=V(7)=5.9211
VG3=V(8)=4.4772
VG4=V(9)=7.5280

The low frequency small signal parameters are:

\[ \beta_{N1} = K_N \frac{W}{L} = (40 \times 10^{-6})(9.6 \times 10^{-6}) = 87.3uA/V^2 \]

\[ I_{DSQ} = 100uA = I_{BIAS} \]

\[ r_{ds1} = r_{ds2} = \frac{1}{\lambda I_{DSQ}} = \frac{1}{(0.02)(100 \times 10^{-6})} = 50 \Omega \]

\[ g_{m1} = g_{m2} = \sqrt{2} \beta_{N1} I_{DSQ} = \sqrt{2}(87.3 \times 10^{-6})(100 \times 10^{-6}) = 132.13 \mu \text{mho} \]
\[ R_{out} = \frac{g_{m2}r_{ds2}r_{ds1}}{2} = \frac{(132.13 \times 10^{-6})(0.5 \times 10^{-6})(0.5 \times 10^{-6})}{2} = 16.52 \text{M} \]

\[ A_{v0} = g_{m1}R_{out} = (132.13 \times 10^{-6})(16.52 \times 10^6) = 2182.78 \]

**Pspice simulation results:**

**** SMALL-SIGNAL CHARACTERISTICS

\[ V(2)/V\text{IN} = -3.136 \times 10^3 \]

INPUT RESISTANCE AT VIN = -2.424 \times 10^{19}

OUTPUT RESISTANCE AT V(2) = 2.342 \times 10^7
6. Cascode Amplifier Design Example
Design specification

Given: $A_V \geq 10,000$  \hspace{1cm} $R_o \geq 10\text{Meg}$

Find: $V_{DD}$, acceptable output voltage swing, and transistor sizing

Design Procedure

$A_V = -g_{m1} R_o$

$g_{m1} = -\frac{A_V}{R_o} = -\frac{10000}{10\text{M}} = -1000\text{umho}$

$R_o = R_{ON}/R_{OP}$

$R_{ON} = R_{OP} = 2R_o$

$R_{ON} \approx g_{m2}r_{o2}r_{o1} = g_{m1}r_{o1}^2 = 2R_o$ \hspace{1cm} $r_{o1} = r_{o2}$

$r_{o1} = \sqrt{\frac{2R_o}{g_{m1}}} = \sqrt{\frac{2R_o^2}{A_V}} = R_o \sqrt{\frac{2}{A_V}} = (10\text{M}) \sqrt{\frac{2}{10000}} = 0.141\text{M}$
\[ r_{o1} = \frac{1}{\lambda I_{DSQ}} \]
\[ I_{DSQ} = \frac{1}{\lambda r_{o1}} = \frac{1}{(0.02)(0.141M)} = 354\mu A \]

\[ g_{m1} = \sqrt{2\beta_N I_{DSQ}} = \sqrt{2K_N (W/L) I_{DSQ}} \]
\[ (W/L)_1 = (W/L)_2 = \frac{g_{m1}^2}{2K_N I_{DSQ}} = \frac{(1000E - 6)^2}{2(40E - 6)(354E - 6)} = 35.3 \]

\[ I_{DSQ} = (\beta/2)(V_{GS} - V_T)^2 = (\beta/2)(\Delta V)^2 \]
\[ \Delta V = \sqrt{\frac{2I_{DSQ}}{\beta}} = \sqrt{\frac{2I_{DSQ}}{K_N (W/L)_1}} = \sqrt{\frac{2(354E - 6)}{(40E - 6)(35.3)}} = 0.708 \]

Output voltage swing neglecting bulk to source effect

\[ V_{TON} + 2\Delta V \leq V_O \leq V_{DD} - (|V_{TOP}| + 2|\Delta V|) \]
1 + 2(0.708) = 2.416 \leq V_O \leq V_{DD} - (1 + 2(0.708)) = V_{DD} - 2.416

2.416 \leq V_{DD} \leq 2.584 \quad ; \quad V_{DD} = 5V \quad \text{(not acceptable)}

2.416 \leq V_{DD} \leq 5.084 \quad ; \quad V_{DD} = 7.5V \quad \text{(acceptable)}

Designing for equal \(\Delta V\) or \(\beta_r=1\)

\[ (W/L)_3 = (W/L)_3 = \frac{K_N}{K_P} (W/L)_1 = \frac{40E - 6}{15E - 5}(35.3) = 94.13 \]

\[ \frac{W_1}{L_1} = \frac{W_2}{L_2} = \frac{W_N}{L_{Neff}} = 35.3 \left( \frac{3}{3} \right) = \frac{105.9L}{3L} \]
\[ \frac{W_3}{L_3} = \frac{W_P}{L_{Peff}} = 94.13 \left( \frac{3}{3} \right) = \frac{282L}{3L} \]

For Lambda \(L=0.6\)

\[ W_N = 105.9L = 105.9(0.6U) = 63.54U \approx 63.6U \]
\[ L_N = L_{Neff} + 2LD = 3L + 2LD = 3(0.6U) + 2(0.5U) = 2.8U \approx 3U \]
\[ W_P = 282L = 282(0.6U) = 169.2U \]
\[ L_P = L_N = 3U \]
*PSpice file for NMOS Common Gate Amplifier with
*PMOS Current Load
*Filename="Lab61.cir"
*All bulks are connected to supply rail
.PARAM Wn=63.6U, Ln=3U
.PARAM Wp=169.2U, Lp=3U
VIN 1 10 DC 0VOLT AC 1V
VDD 3 0 DC 7.5VOLT
VSS 4 0 DC 0VOLT

M1 5 1 4 4 NMOS1 W={Wn} L={Ln}
M2 2 7 5 4 NMOS1 W={Wn} L={Ln}
M3 2 8 6 3 PMOS1 W={Wp} L={Lp}
M4 6 9 3 3 PMOS1 W={Wp} L={Lp}

*Biasing circuit
MBN1 10 10 4 4 NMOS1 W={Wn} L={Ln}
MBN2 7 7 10 4 NMOS1 W={Wn} L={Ln}
IBP 8 4 354UA
MBP1 8 8 9 3 PMOS1 W={Wp} L={Lp}
MBP2 9 9 3 3 PMOS1 W={Wp} L={Lp}
MBP3 7 8 11 3 PMOS1 W={Wp} L={Lp}
MBP4 11 9 3 3 PMOS1 W={Wp} L={Lp}

.MODEL NMOS1 NMOS VTO=1 KP=40U
+ GAMMA=1.0 LAMBDA=0.02 PHI=0.6
+ TOX=0.05U LD=0.5U CJ=5E-4 CJSW=10E-10
+ U0=550 MJ=0.5 MJSW=0.5 CGSO=0.4E-9 CGDO=0.4E-9
.MODEL PMOS1 PMOS VTO=-1 KP=15U
+ GAMMA=0.6 LAMBDA=0.02 PHI=0.6
+ TOX=0.05U LD=0.5U CJ=5E-4 CJSW=10E-10
+ U0=200 MJ=0.5 MJSW=0.5 CGSO=0.4E-9 CGDO=0.4E-9

*Analysis
.DC VIN -2.5 7.5 0.05
.TF V(2) VIN
.AC DEC 100 1HZ 10GHZ
.PROBE
.END

**** SMALL-SIGNAL CHARACTERISTICS

V(2)/VIN = -1.268E+04
INPUT RESISTANCE AT VIN = -1.318E+19
OUTPUT RESISTANCE AT V(2) = 1.321E+07

NODE VOLTAGE NODE VOLTAGE NODE VOLTAGE NODE VOLTAGE

( 1) 1.7334 ( 2) 4.2146 ( 3) 7.5000 ( 4) 0.0000
( 5) 1.7334 ( 6) 5.7694 ( 7) 4.2146 ( 8) 3.5826

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The circuit is simulated with VDD=5V to show that the resulting cascode does not yield the desired gain and output impedance. Replace the VDD line in the netlist to:
VDD 3.0 DC 5VOLT

**** SMALL-SIGNAL CHARACTERISTICS

V(2)/VIN = -1.216E+01

INPUT RESISTANCE AT VIN = 3.651E+18

OUTPUT RESISTANCE AT V(2) = 1.285E+04

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