Lab 7: Schematic Capture Using Virtuoso Schematic Editor (VSE)

This Lab will go over:

1. Logging in
2. Setting up your account
3. Design Entry through schematic capture
4. Compiling a new project directory
5. Creating nand2 schematic view
6. Creating nand2 symbol view

1. Logging in

Cadence tools can be accessed from these locations: Engg2360, Basement of Science and Engineering library, Engg3337, and Engg2351.

LOGGING IN FROM AN XTERMINAL IN Engg 3337

At the CDE (Common Desktop Environment) login window type your login id followed by ENTER and then type your password followed by ENTER.

If asked what interface to use we recommend you choose CDE. If you ever want to change your login "session" you may do so by selecting the OPTIONS button on the login window and choose a session listed in the Sessions Menu (CDE, OpenWindows).

LOGGING IN FROM A SPARCSTATION in Engg2360 and Basement of Science and Engineering Library

At the CDE (Common Desktop Environment) login window first go to OPTIONS -> REMOTE LOGIN and then type emitsun1. After this the procedure is the same as using an xterminal. (see above).
LOGGING IN FROM A PC USING EXCEED IN ENGG 2351

Log in the pc, then go to Start > Programs>Exceed>Exceed(XDMCP-Broadcast), a hostname list will show up, select emitsun1 from the list and click ok. An emitsun1 login window will come out. After this the procedure is the same as using an xterminal. (see above)

2. Setting up your account:

Your account should have the all paths set to run the software. You need only to log in and start a terminal. There should be a terminal icon on your Common Desktop Environment. Just double click on it and a command window will appear. If no terminal icon is available, you can open a new terminal by right clicking the mouse button on the workspace area and select Programs>Terminal… or Programs>Console…. To setup your environment type the following commands:

emitsun1% cd --to go to home directory, if not in home directory
emitsun1% mkdir cell --create the project directory under your home directory
emitsun1% cd cell -- go to project directory
emitsun1% ls --list the files in the project directory, you should see no files
emitsun1% icfb & --start CDS tools under your project directory

“&” means start CDS tools in the background mode, so that the command window is still available for entering UNIX commands.

Figure 1 shows the sequence of commands mentioned above. After some time, the CIW (Command Interface Window) will pop up (Figure 2). Once the CIW come up you will not need to use the UNIX command line.

Figure 1: Starting CDS tools (icfb-IC Front to Back)
3. Design entry through schematic capture:

This is the beginning of the design flow as far as using CDS tools is concerned. Prior to starting the tools you need to have define your logic function, decided on an implementation, reduced the number of gates, and done some initial sizing of the lengths and width of your transistors.

Now that you have created your project directory, whenever you want to work on the design in that directory you just have to:

1. Log in
2. Start a terminal
3. Type in the command, `cd cell` (or the name you selected for your project)
4. Type in the command, `icfb &`.

We will be using the NCSU design kit, which automatically starts the library manager (Figure 3.) You should see three NCSU libraries and a library named basic, `cdsDefTechLib`, and `ami06_stdcell`. 
4. Compiling a new project directory:

We need to create a project library and compile a technology library to it. The tech library contains all the process specific information needed to design an IC using a particular fabrication house’s process. We will be using AMI 0.6u ABN (3M, 2P, high-res) process. This process has 3 metal layers (3M), 2 polysilicon layers (2P) and a high resistance layer (high-res), which dope the second polysilicon layer to increase its resistivity.

To compile your new project library:

1. Go to Library Manager and execute: (LM)File>New>Library…. A pop-up like Figure 4 should appear.

2. Fill out the pop up exactly according to Figure 4. Make sure to click on “Attach to existing tech library”.

3. Click OK. You should see messages in the CIW similar to the ones in Figure 5.
4. Your library manager should now show your new project directory in column 1, as in Figure 6. Also, make sure when you click on NCSU_TechLib_ami06 library that it has all the components listed in column 2 of Figure 6.

Figure 4: Creating a Library

Figure 5: CIW messages while creating a library
5. Creating nand2 schematic view:

After creating the library AMI06, we can now start adding our circuit views. Each circuit will have different views. For example, our nand2 will have a schematic, symbol, layout, and extracted views. There are more views than these, but these are the only ones we will use in this course.

1. Schematic view: The circuit is described by electronic symbols connected by wires. A spice run deck can be compiled directly from this view. For example, a nand2 would have four transistors, a power supply, ground, and 2-input and 1-output ports.

2. Symbol view: The circuit is described by one symbol. For example, a nand2 would look like the Boolean logic symbol for a 2-input nand gate.

3. Layout: The circuit is drawn, as it would appear if you looked at it under a microscope. Each drawn layer corresponds to a process step, which follows a design rule.

4. Extracted: CDS tools can extract a schematic from the drawn layers. This is helpful to make sure you drew the circuit so that it will perform like the schematic. The extracted
view will include parasitic components such as capacitances and resistances from the drawn layers that the schematic view cannot generate.

To create a schematic view:

1. Go to the library manager and execute: (LM)File>New>Cellview…. A pop-up like Figure 7 should appear.

2. Fill out the pop-up exactly according to Figure 7.

3. Click OK. The schematic entry tool should appear (Figure 8).
Figure 8: The schematic capture tool.

The schematic capture tool will be used to draw the schematic representation of your nand2.

To draw the nand2 you need to add 2 pmos transistors, 2 nmos transistors, 2 power pins, 2 input pins, 1 output pin, and wire them together.

To add items to your schematic go to composer tool and execute \textit{(VSE)Add>Instance...}, or press the letter \textit{i}. The add instance pop-up appears like in Figure 9.

Click on \textbf{browse} button to graphically get components. A pop-up like Figure 10 should appear.
To get the parts we need change the library to **NCSU_Analog_Parts** according to Figure 10. This figure shows the category of various components. You need to know the component category to retrieve the parts.
Click on **Flatten** to see all the components listed in alphabetical order, the pop-up should look like Figure 11.

![Component Browser](image)

**Figure 11**: Getting vdd and gnd.

To add the transistors click on the nmos4 and pmos4 in the component browser. These are 4-terminal transistors where the bulk connection is manually connected to gnd for nmos4 and vdd for pmos4. The pop-up for the nmos4 should look like Figure 12, and the pmos4 pop-up should look like Figure 13. From the pop-up change the width and length: W=6u and L=600n for nmos4; and W=7.2u and L=600n for pmos4. Stamp two nmos4 and two pmos4 as shown in Figure 16.
Figure 12: Getting an nmos4 terminal device
To add the input pins, execute (VSE)Add>Pin… A pop up like Figure 14 should appear. Fill it out exactly like Figure 14. The pins names must match the pins names of the symbol view we are going to create later. If they do not match (direction or name), the design, check & save routine will fail.
To add the output pin Y follows the pop-up shown in Figure 15. Stamp it down as shown in Figure 16. It does not have to be exact but neatness will help further.

If you make a mistake and need to get out of add instance mode, press the ESC key.

Click on the object you want to delete and press the del key.
All that remains to be done is to wire the connections together. To add a wire, press w. The wire will snap to place at the proper ports of each device. Click once to start wiring, and single click to end it. Proceed wiring the remaining connections. Wire it up like Figure 17.
To save and check your schematic for errors, execute (VSE)Design>Check and Save. Any errors will be highlighted in the schematic window. Usually something is not connected, or a port name is wrong.

6. Creating a symbol view:

To create a symbol view:

1. Go to the library manager and execute (LM)File>New>Cell View…. A pop-up like Figure 18 should appear.
2. Fill out the pop up exactly according to Figure 18. Click OK. The symbol editor tool should appear (Figure 19).
The symbol editor allows you to draw any kind of shape to represent your logic gate. The important part is to have the input and output pins match whatever it is you are representing. In this case, we need to match the input pin A, B, mygnd, myvdd, and output pin Y of the nand2. Rather than drawing a nand2 symbol from scratch, it is much easier to copy one that has already been drawn.

To import a symbol:

1. Go to symbol editor and execute (VSbE)Add>Import Symbol…. A pop-up like Figure 20 should appear. Click on browse and select the nand2 in the digital library of the NCSU kit. The pop-up should look exactly like Figure 20.

2. Stamp it down in the symbol editor like in Figure 21.

3. Press the ESC key to get out of add symbol mode.

4. Press the f key to fit the symbol in your window.

Figure 20: Importing a symbol
Figure 21: The nand2 symbol

The standard nand2 symbol does not provide the power pins; vdd, and gnd. The vdd and gnd are global signals. Global signal are automatically given pins. This makes our symbols cleaner because we only show logic ports. However, we found out the layout circuit extraction does not work if we don’t explicitly provide local power pins: myvdd and mygnd. These pins are then connected to vdd and gnd in the test bench for simulation. To add the power pin myvdd, copy a pin (say the input pin A) change the name, rotate, and move as shown in Figure 22. Similarly add mygnd as shown in Figure 22.

To copy a pin and its label (say pin A) do the following:

1. Select pin A and its label, then execute (VSbE)Edit>Copy.

2. Click once to copy, then move a ghost image will follow the cursor, click once to placed it down.

To change the pin name, do the following:
1. Select the copied pin A and its label (it should already be selected), then execute (VSB) Edit > Properties > Objects…. A pop-up will appear change the label to myvdd. Click OK. A warning message will display:

*Pin label “A” is renamed to “myvdd”. NOTE: that the label not associated with a pin. The actual pin name has not been changed.*

2. To rename the pin, first unselect the copied pin A and its new label, then select the pin only, and execute (VSB) Edit > Properties > Objects…. A pop-up will appear, change the name to myvdd.

**To rotate the pin and its label**, do the following:

1. Select the pin and its label, then execute (VSB) Edit > Move…. A pop-up will display, showing the following options: Rotate (rotate 90° CCW), Sideways (to flip horizontally), Upside Down (to flip vertically).

2. Apply the options needed to achieve the desired orientation of the pin, as shown in Figure 22.

3. Select the label only, then move and rotate as shown in Figure 22.
When you are done save your symbol by executing (VsbE)Design>Check & Save. You should have no errors. If there are errors, the pins must be wrong in your schematic. Go back to your schematic and fix the pin assignments. Check for direction and name. If there is one pin misnamed there will be two errors:

1. A pin in the schematic view was not found in the symbol view.
2. A pin in the symbolic view was not found in the schematic view.

To close the symbol editor, go to (VsbE)Window>Close.
Assignment:

1. Create the schematic diagram for inverter (inv), as in Figure 23.

2. Create the inv symbol as in Figure 24.

You will need the inverter (inv) when we create the exclusive-or (xor2) in Lab 5.

Figure 23: Inv schematic diagram.
Figure 24: Inv symbol with local power pins